ECLIPSE SYSTEM OVERVIEW

MICROTEST
Equipment & Consumables for the semiconductors and hybrids

- MRC Technology
- System Overview
- Equipment Details
- Process Performance
- Summary

TFE
Thin Film Equipment

ECLIPSE PROCESS CAPABILITY

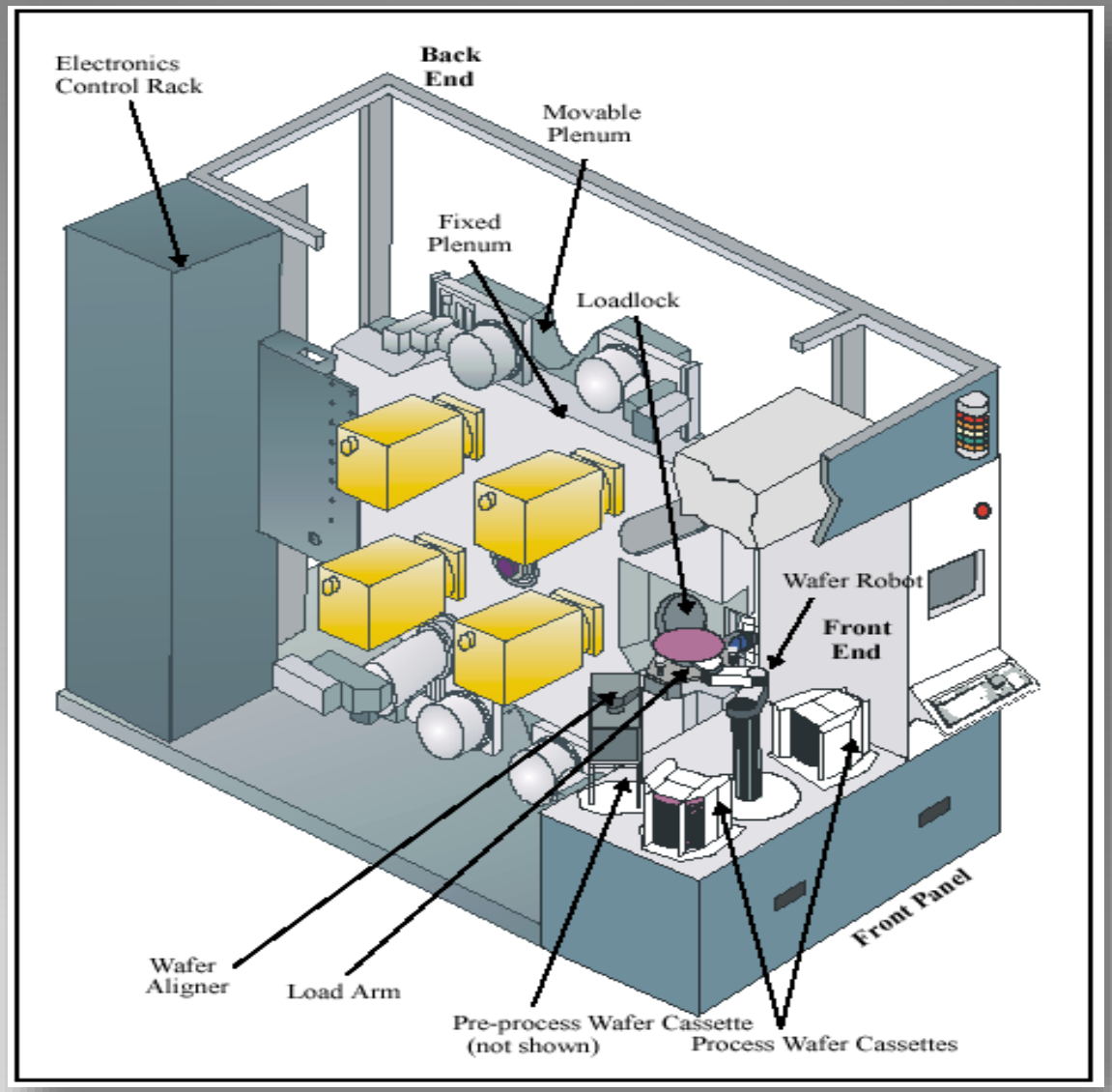
- Interconnects
  - **Ti/TiN/Al/TiN**
  - **Hot Al for Via Fill**
- Barriers
  - **TiN and TiON**
  - **TiW and TiWN**
- Silicides
  - **Ti, Co, Pt**
- Resistors and Conductors
  - **Ta, TaN, Ta/Au, TaAl**
  - **NiCr, SiCr, Si**
- Backside and GaAs
  - **Ni, NiV, Cr, Cu, Au, Ag, ...**

ECLIPSE KEY FEATURES

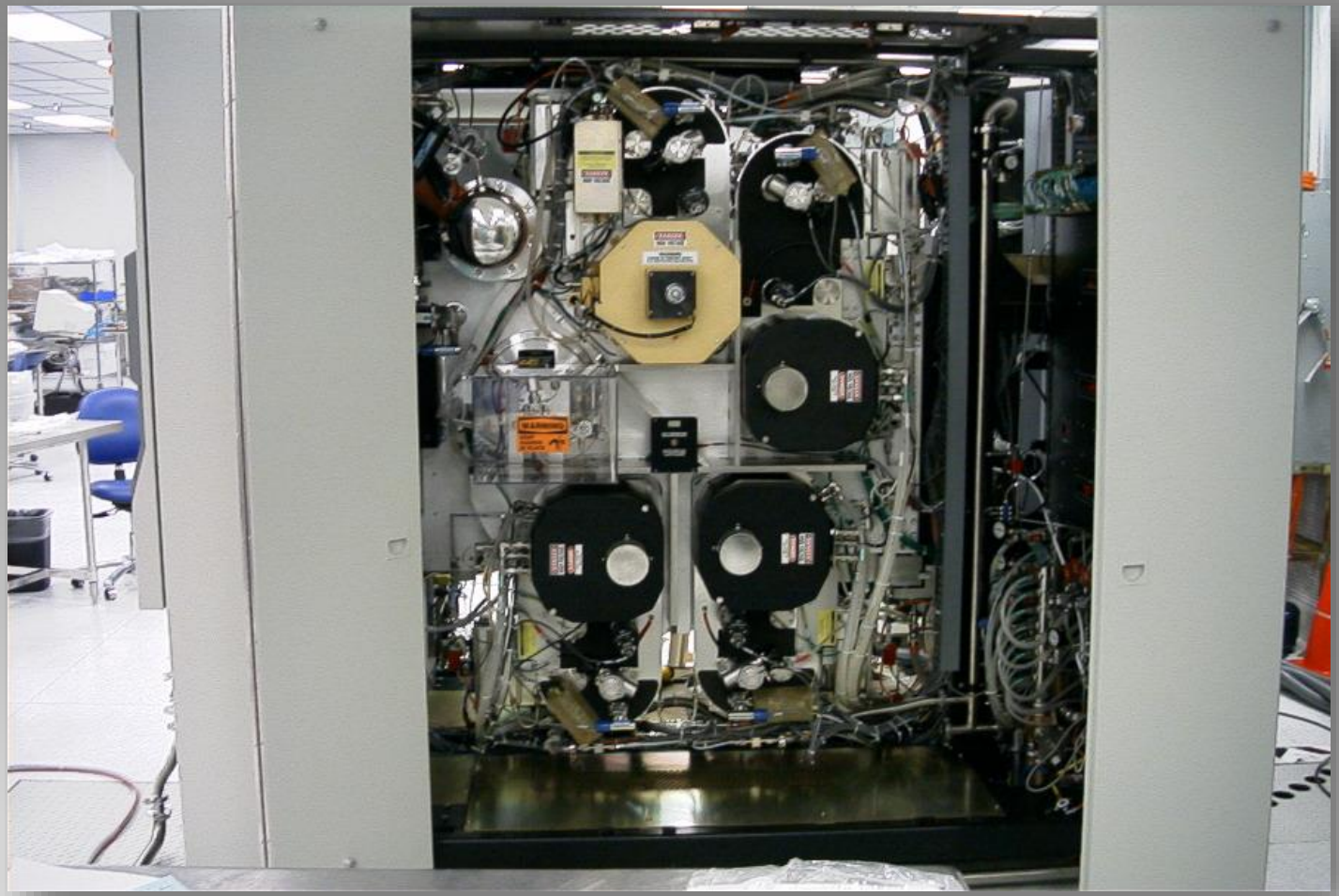
MICROTEST
Equipment & Consumables for the semiconductors and hybrids

- High Throughput
  - **48 WPH (1um Al Deposition)**
  - **Serial Indexed Wafer Transport**
- Superior Process Control
  - **Vacuum Isolated Process Chambers**
  - **Rotating Magnet Cathodes**
  - **Process Specific Shield Designs**
  - **Reactive N_2 and O_2 Sputter Capability**
  - **GaAs and Backside Processing Available**
- Reduced Maintenance
  - **Quick Clamp Exchange**
  - **Rapid Target Change**
  - **On-Board CTI Fast Regen Cryo Pumps**
  - **Proven 150mm Platform ~900 in field**

TFE
Thin Film Equipment



ECLIPSE STAR MOVEABLE PLENUM VIEW



Thin Film Equipment

ECLIPSE – Wafer Handler

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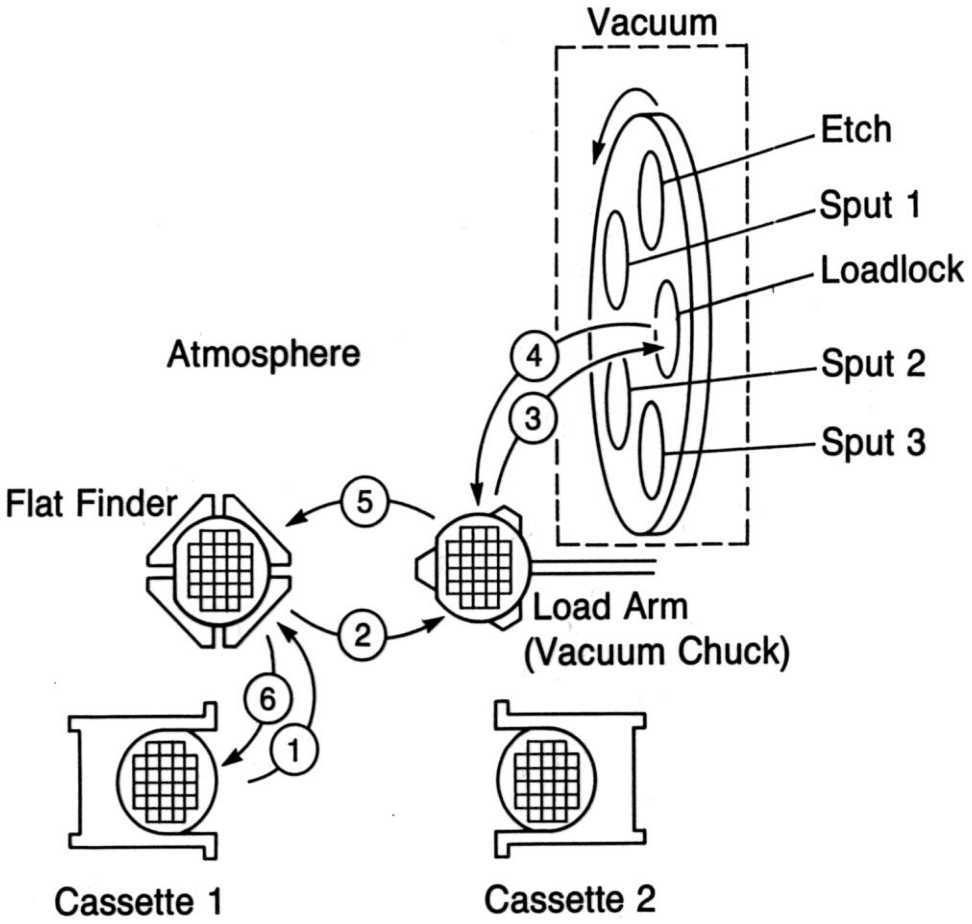
Equipment & Consumables for the semiconductors and hybrids

Features

- Robotic Pick and Place Wafer Handler
- Dual Cassette Elevators
- Optical Flatfinder
- Centering Station
- Optional Preprocess Cassette

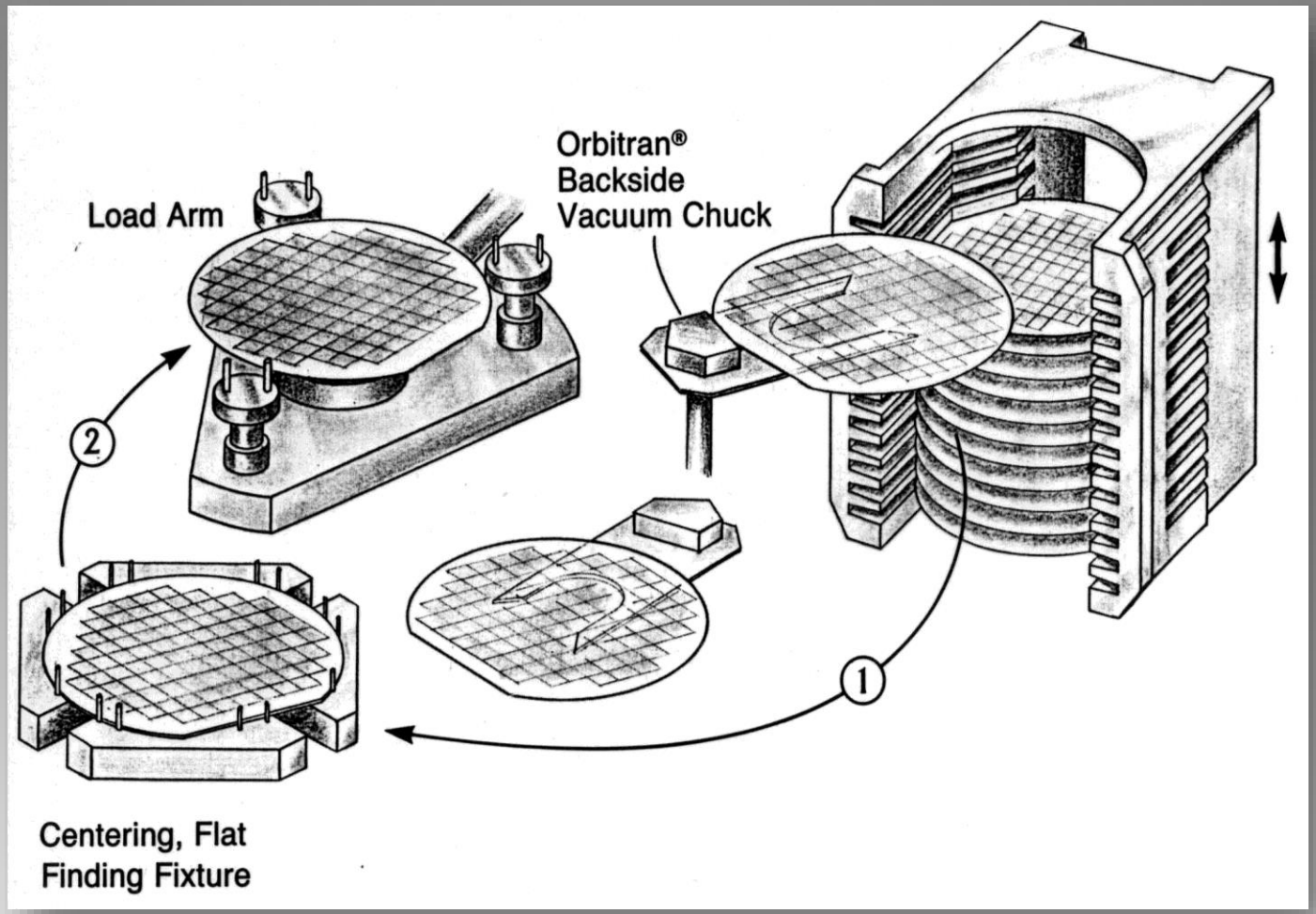
TFE
Thin Film Equipment

Wafer Hand-Offs

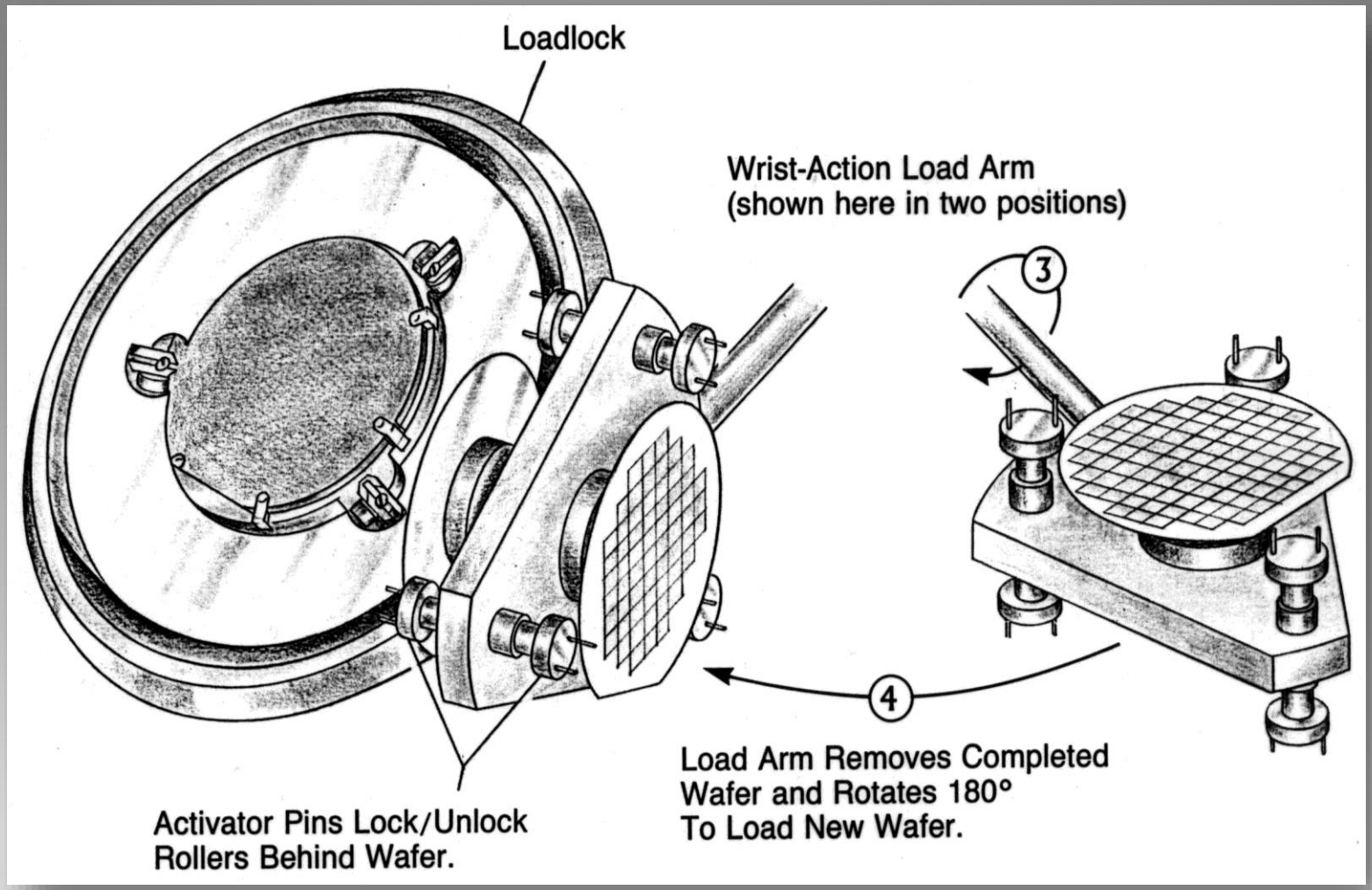


- Wafers transported horizontally in atmosphere
- Load arm converts wafer position to vertical before processing and back to horizontal after processing
- Single Orbitran® mechanism transfers wafers between cassette, flat finder, and load arm
- Wafer - wafer integrity maintained in cassettes

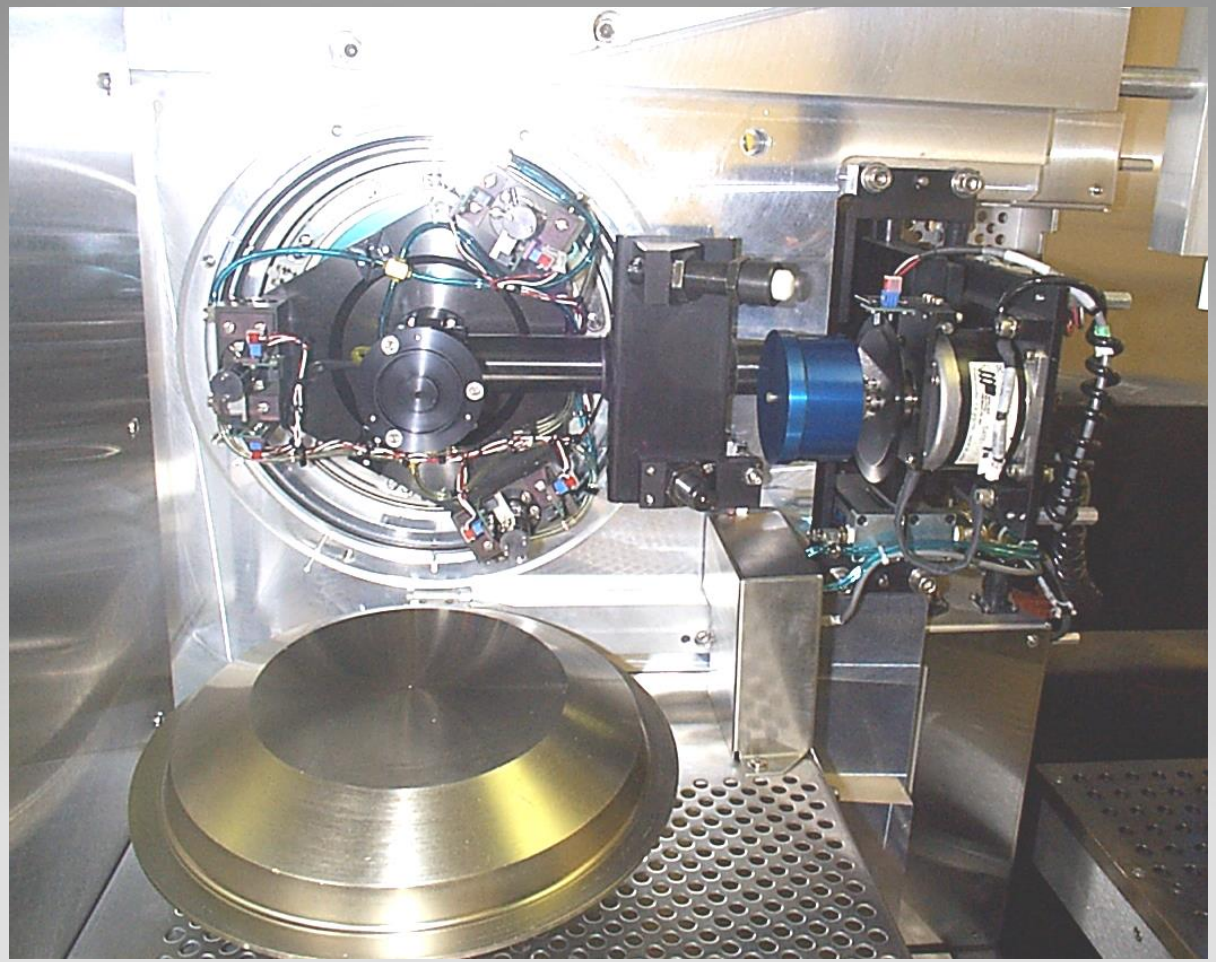
Wafer Loading 1 Cassette – Load Arm



Wafer Loading 2 Load Arm - Loadlock



Wafer Handling into Loadlock



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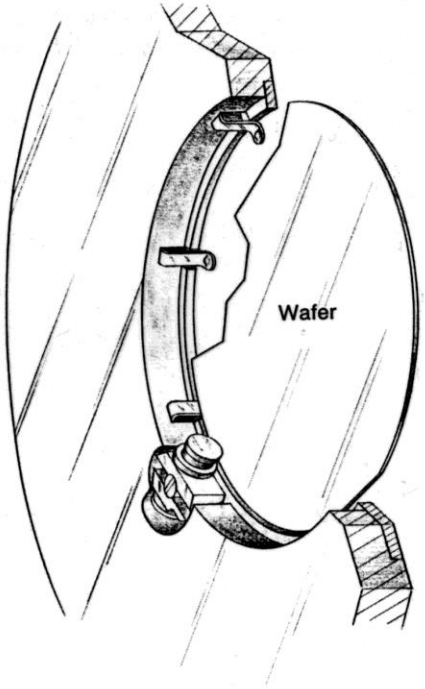
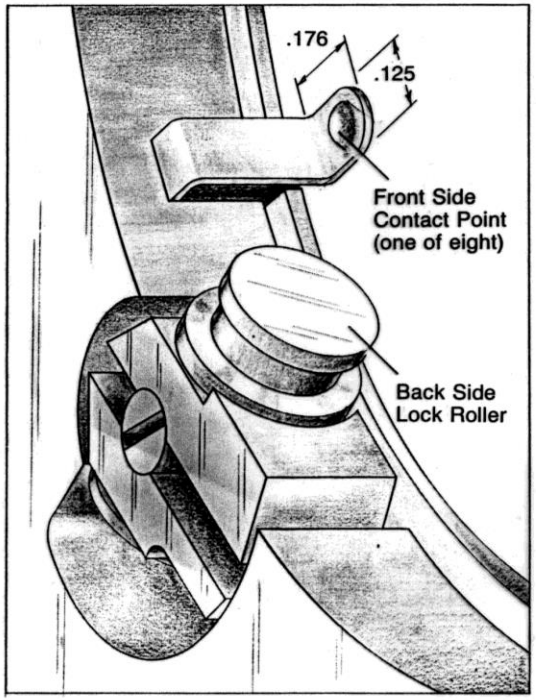
Wafer Loading 3 Wafer Holder



Backside View of Wafer in Load Lock

- Wafer held securely in wafer holder
  — vertical during all processing
- No wafer motion during all processing



Wafer Holder Assembly

- Compliant tabs maintain consistent wafer contact pressure
- Wafer holder design reduces particulates during deposition
  — No moving parts in vacuum
  — Roller contacts backside of wafer over a distance of 0.045 in
  — No edge contact

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Equipment & Consumables for the semiconductors and hybrids

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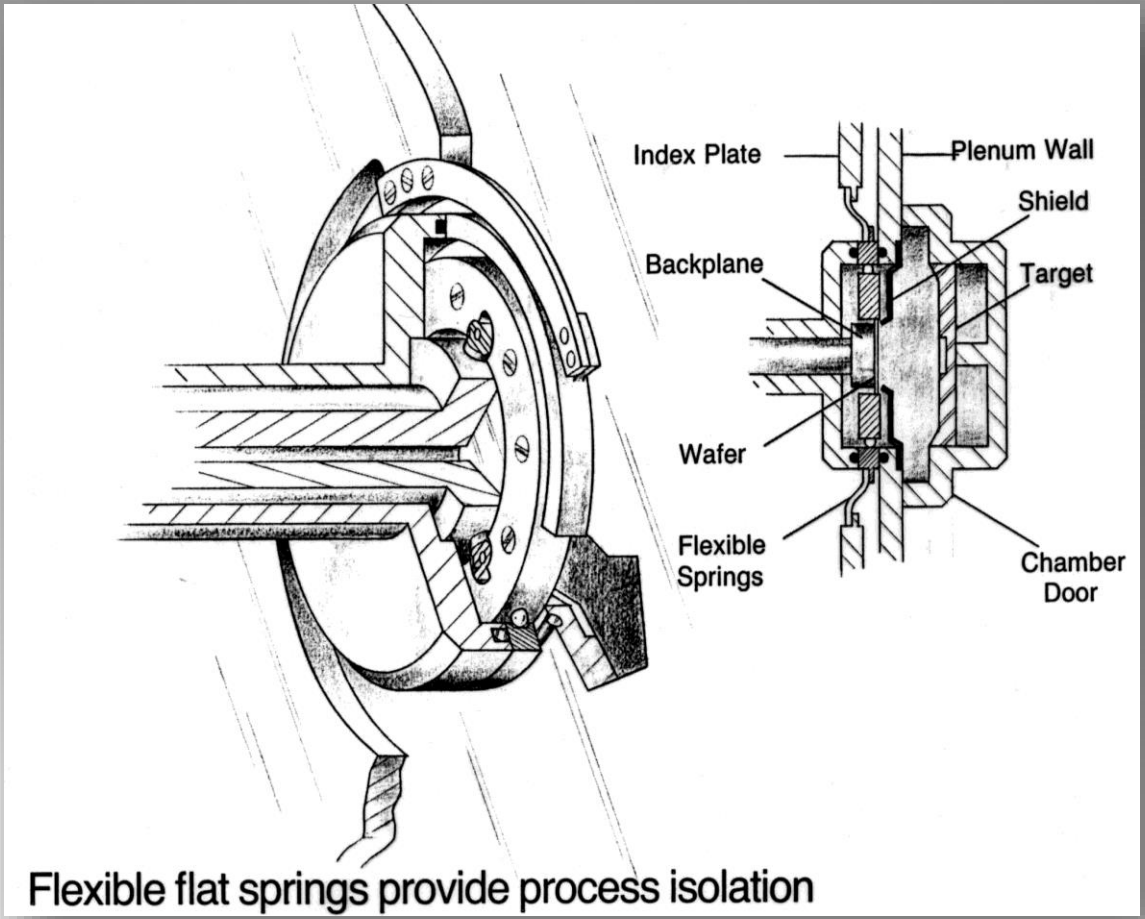
Wafer Isolation 2 - Sealed



Flexible flat springs provide process isolation

MICROTEST
Equipment & Consumables for the semiconductors and hybrids

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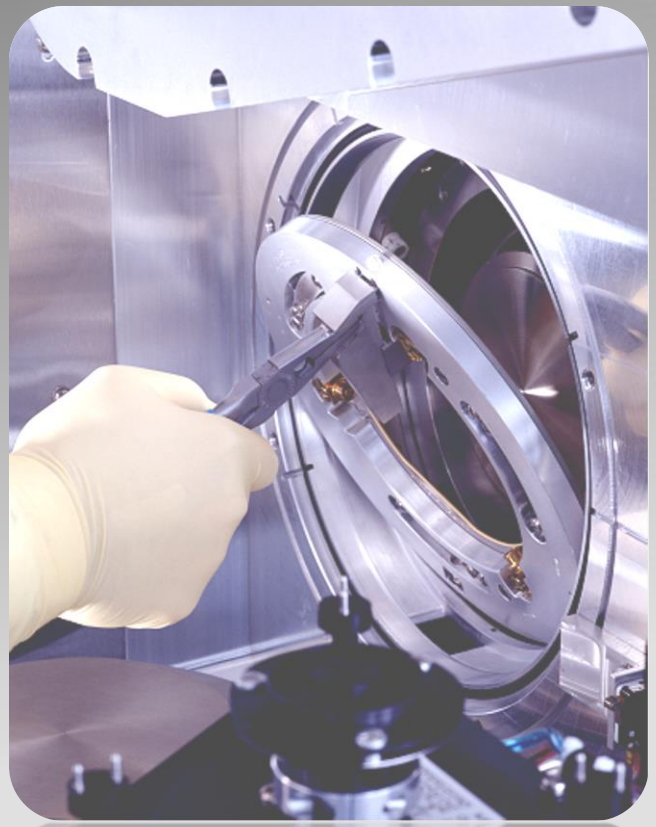
Thin Film Equipment

Quick Clamp Exchange



- Full circumference 1.5mm edge exclusion
- Standard fully ceramic latch assemblies (body & roller)
- Low particulate cam action latching
- Six self-aligning screws for easy maintenance
- Full system exchange in less than 30 min.
- Specially designed for the new round backplane (reduces secondary plasmas)

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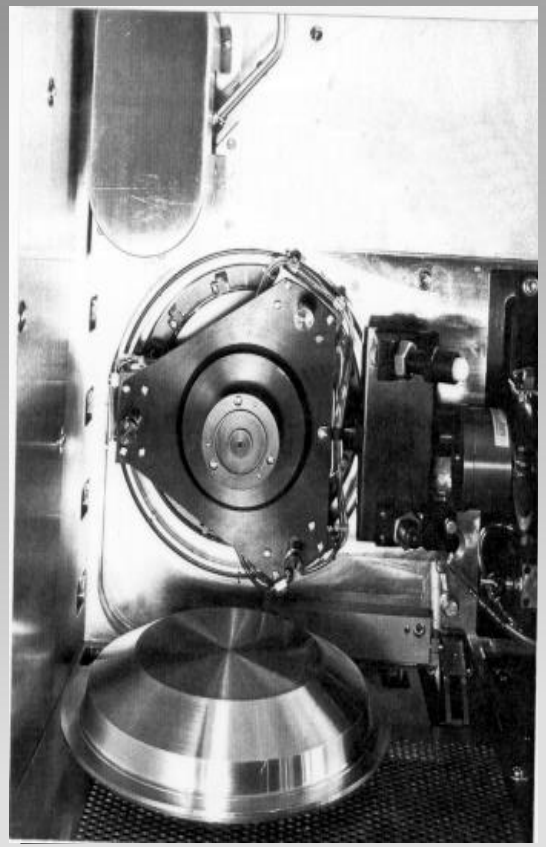
MICROTEST
Equipment & Consumables for the semiconductors and hybrids

Vacuum Loadlock



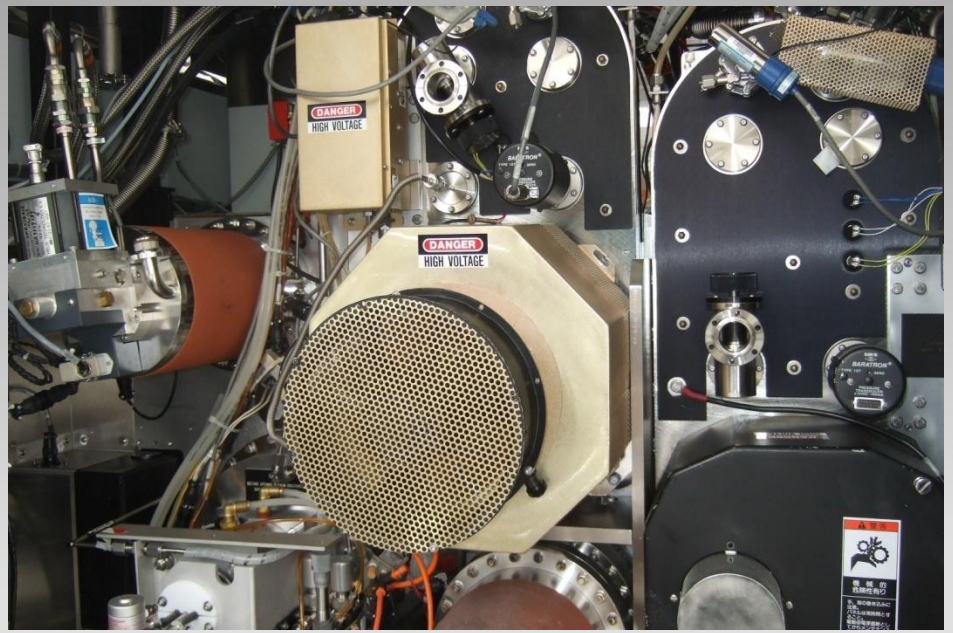
- Dedicated CTI-8 Cryo Pump
- Radial Slow Vent for Low Particle Generation
- Heated Frontplane up to 200C for Outgassing
- Dual Sided Loadarm For High Throughput
- Quick Clamp Exchange

TFE
Thin Film Equipment

ICP Soft Etch Module option

- Pre-clean sputter etch of native oxides
- Inductively Coupled Plasma (ICP)
  - Offers high density plasma with independently controlled wafer bias
  - The quartz process chamber has a special surface treatment to improve material adhesion
- Improved Yield
  - Low device damage
- Increased Throughput
  - High etch rate (100-600 Å/min)

Soft Etch



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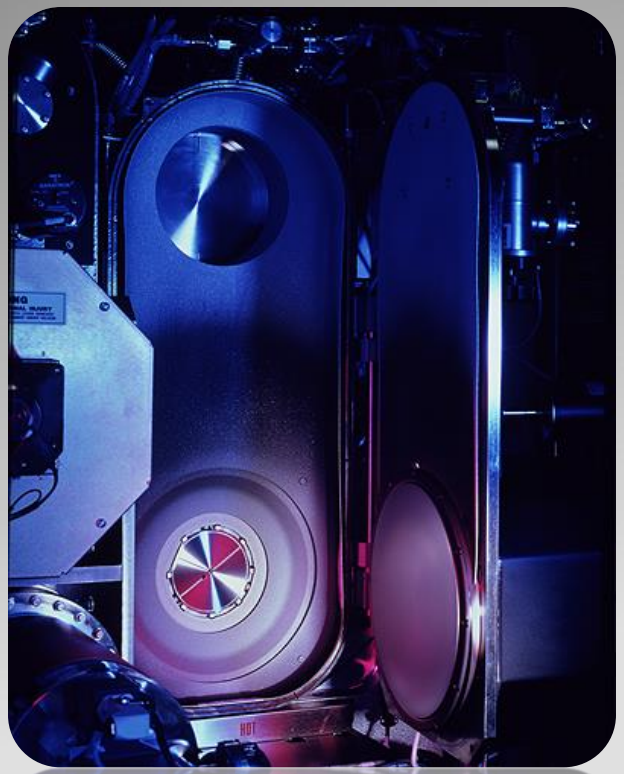
PVD Process Chamber

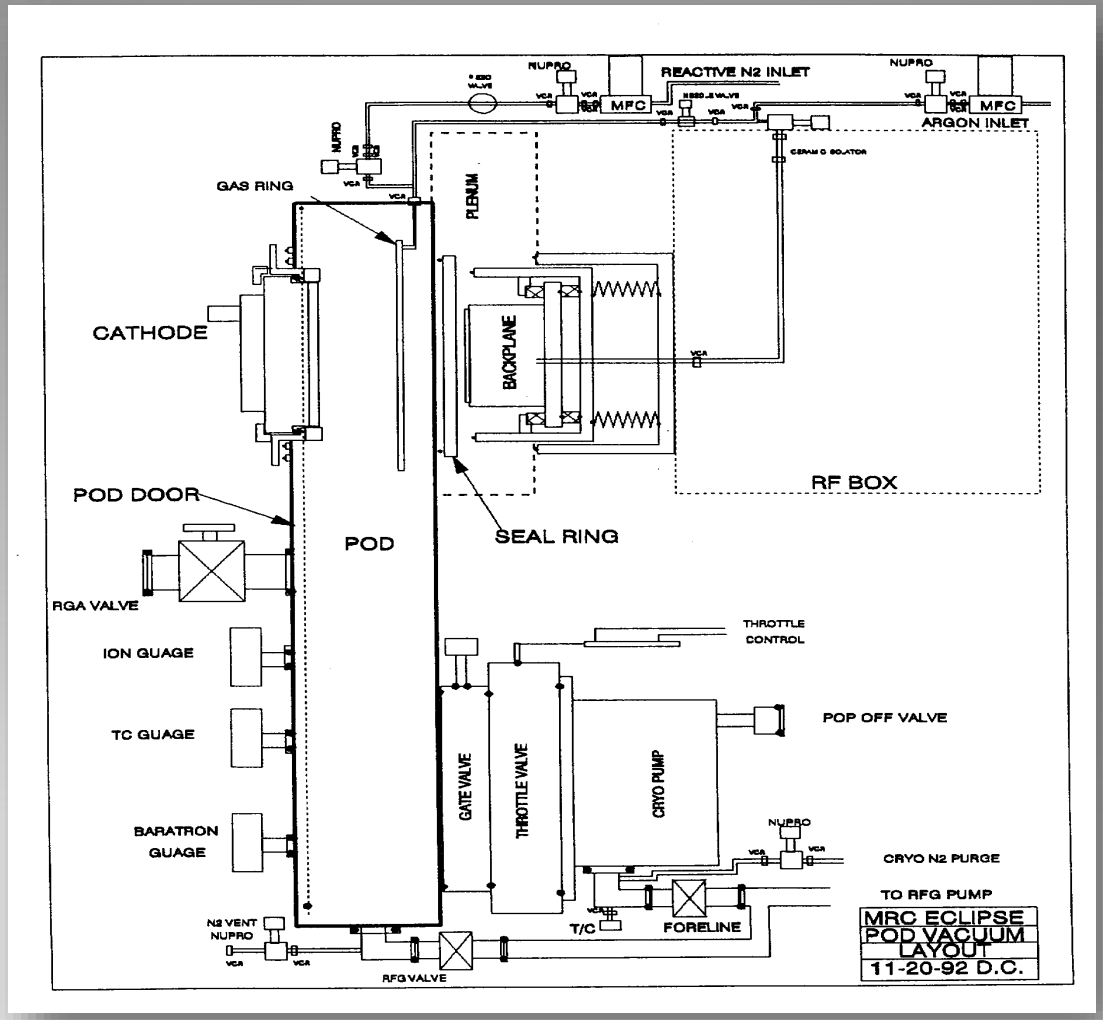


- Three Metal Process Capability
- Full Face Erosion Magnetron Technology
- Hard Etch std-Soft Etch option
  - RMX-10, SPA-10 - Standard
  - RMX 12”, SPA 12”- option
- Reactive N2 and O2 option
- RF BIAS option

Thin Film Equipment

ECLIPSE ®

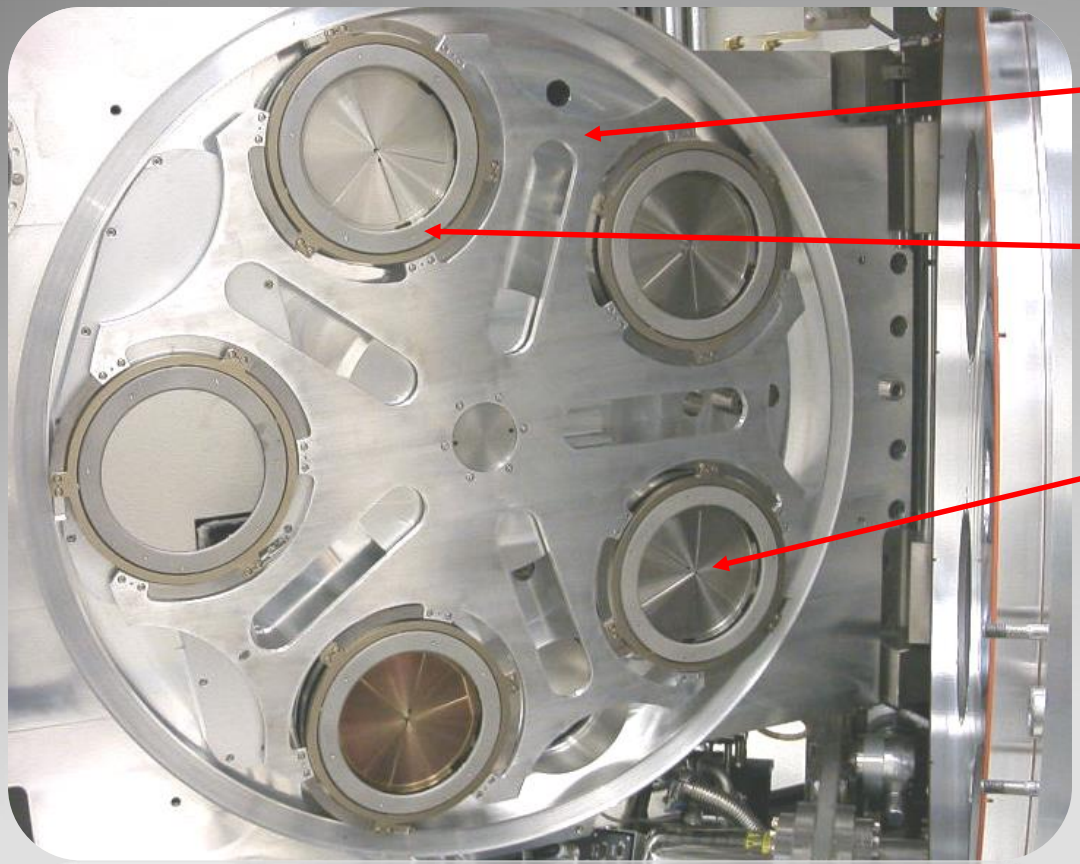
Pod and Backplane



Thin Film Equipment

ECLIPSE ®

Wafer Transport Module



Index Wheel

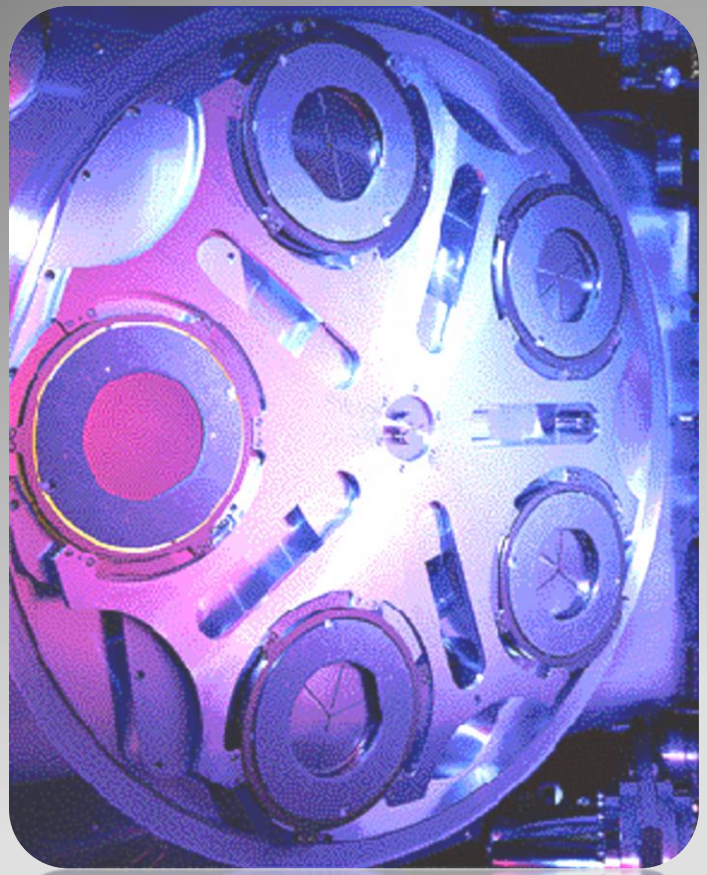
Wafer Holders,
five places

Backplanes

Thin Film Equipment

ECLIPSE ®

Wafer Transport Module

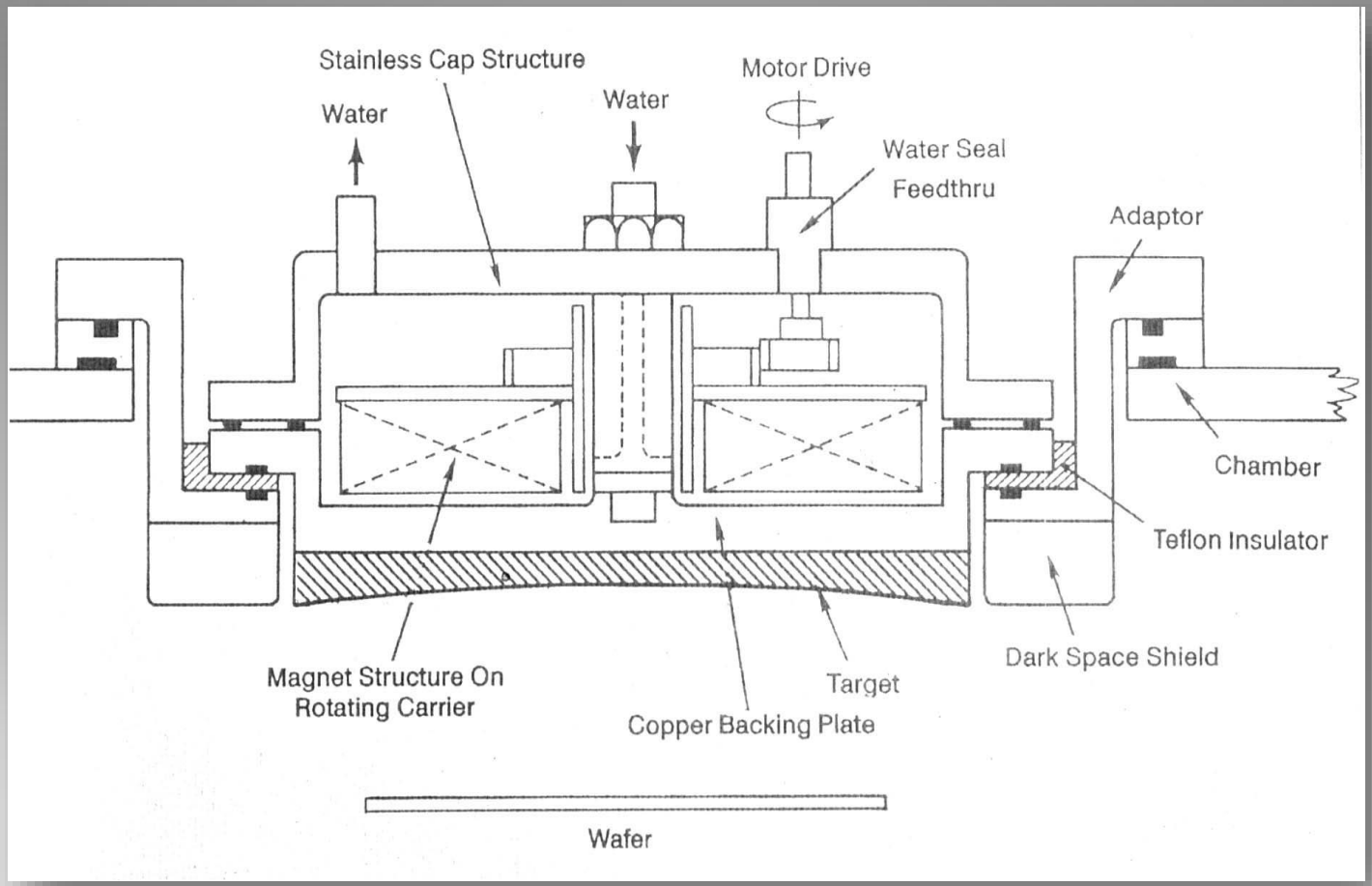


- **High Speed Serial Indexed Wafer Transport**
- **Precision Index Wheel Positioning**
- **Full Face Clamp Ring Wafer Holders**
- **Wafers are Clamped once during Transport through all Chambers**
- **No Sputtering on the Backplanes or Backside of the Wafer**

TFE
Thin Film Equipment

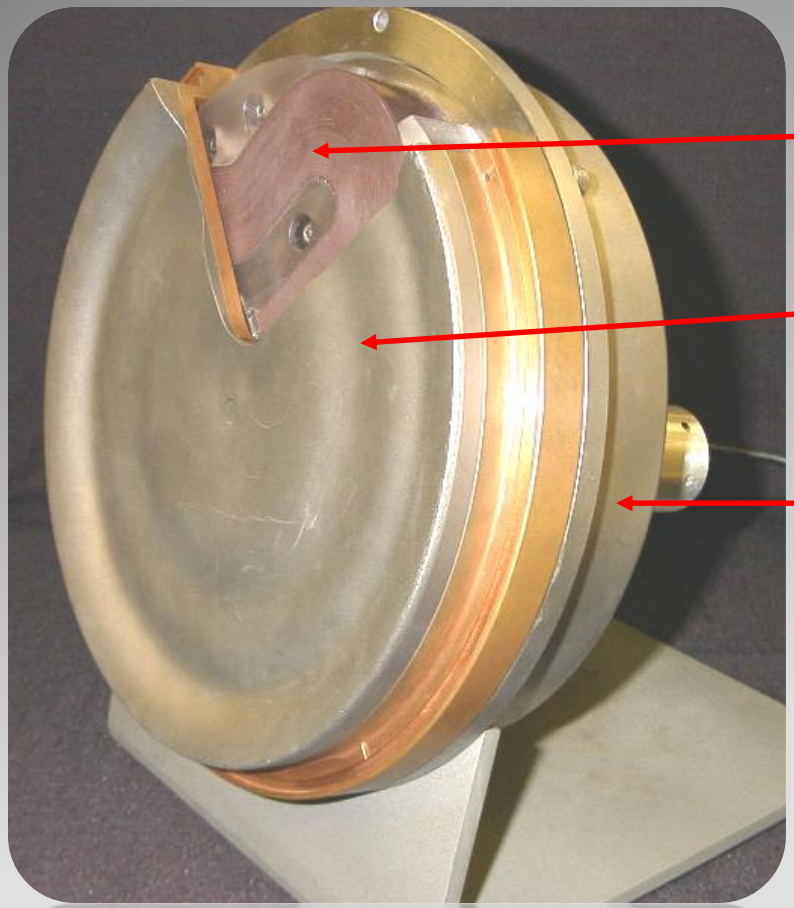
ECLIPSE ®

RMX Cathode Schematic



Thin Film Equipment

Cathode/Target Cut Away



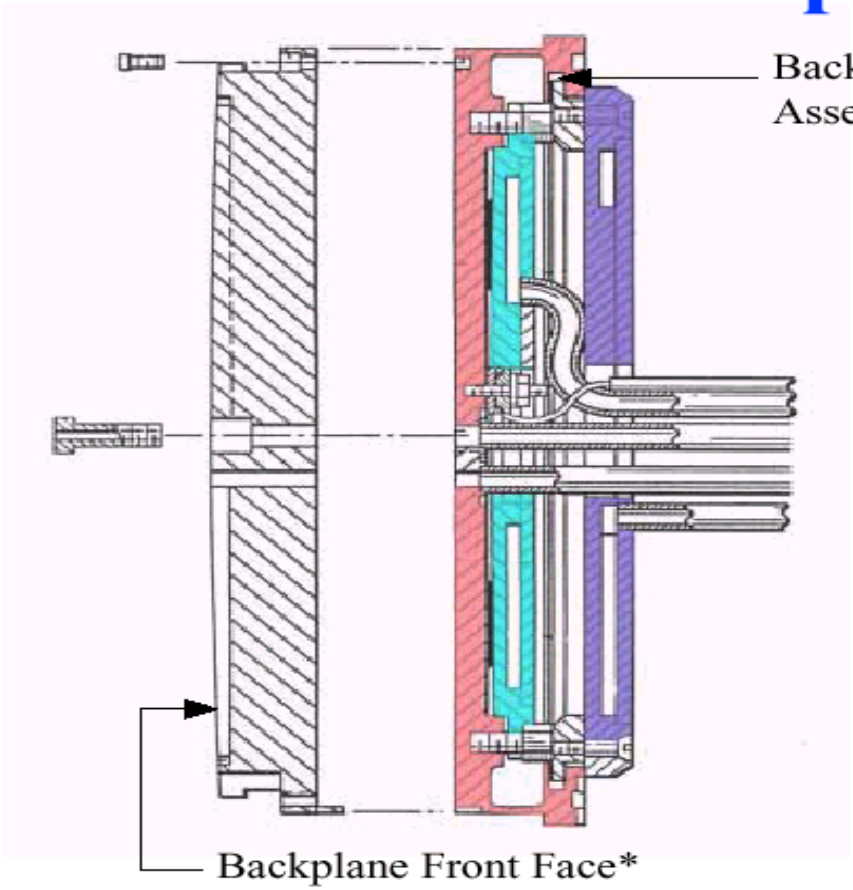
- Rotating Magnet Assembly
- Target Assembly
- Cathode Housing

ECLIPSE Wafer Temperature

- **Control is achieved by using backside gas**
  - **Heat source (bring wafer temp. up/down)**
  - **Heat sink (hold wafer temp. during dep.)**
- **Without control, deposition of 1 µm of Al**
  - **raises wafer temperature by 250 - 550 C**
  - **wafer is only inefficiently cooled by radiation**
- **Understanding of the mechanism is key for**
  - **successful process design on the Eclipse**
  - **successful process move from/to „other“ equipment**

Thin Film Equipment

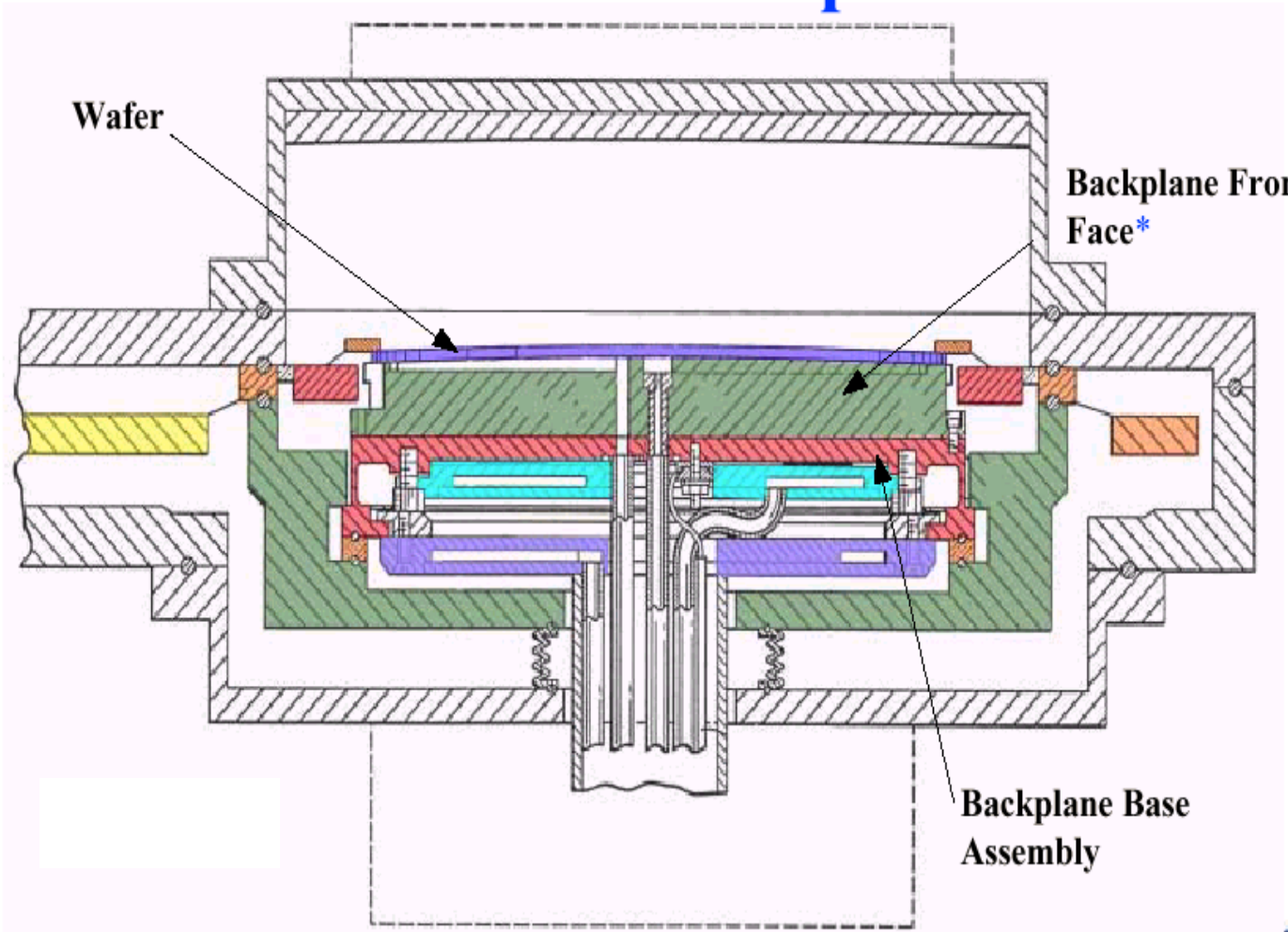
Universal Backplane



* Wafer Size Dependent

PEOPLE. TECHNOLOGY.

Universal Backplane



* Wafer Size Dependent

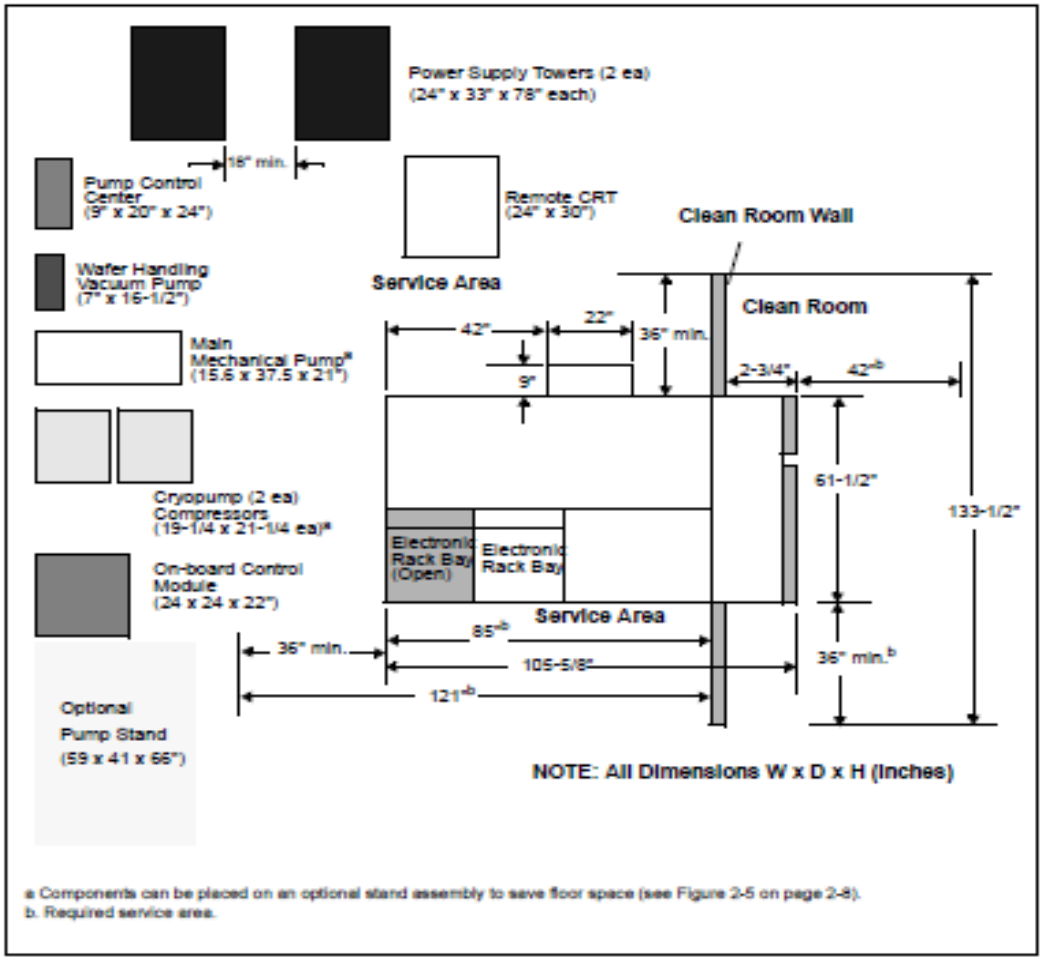
Control of Stress

CONTROL OF STRESS

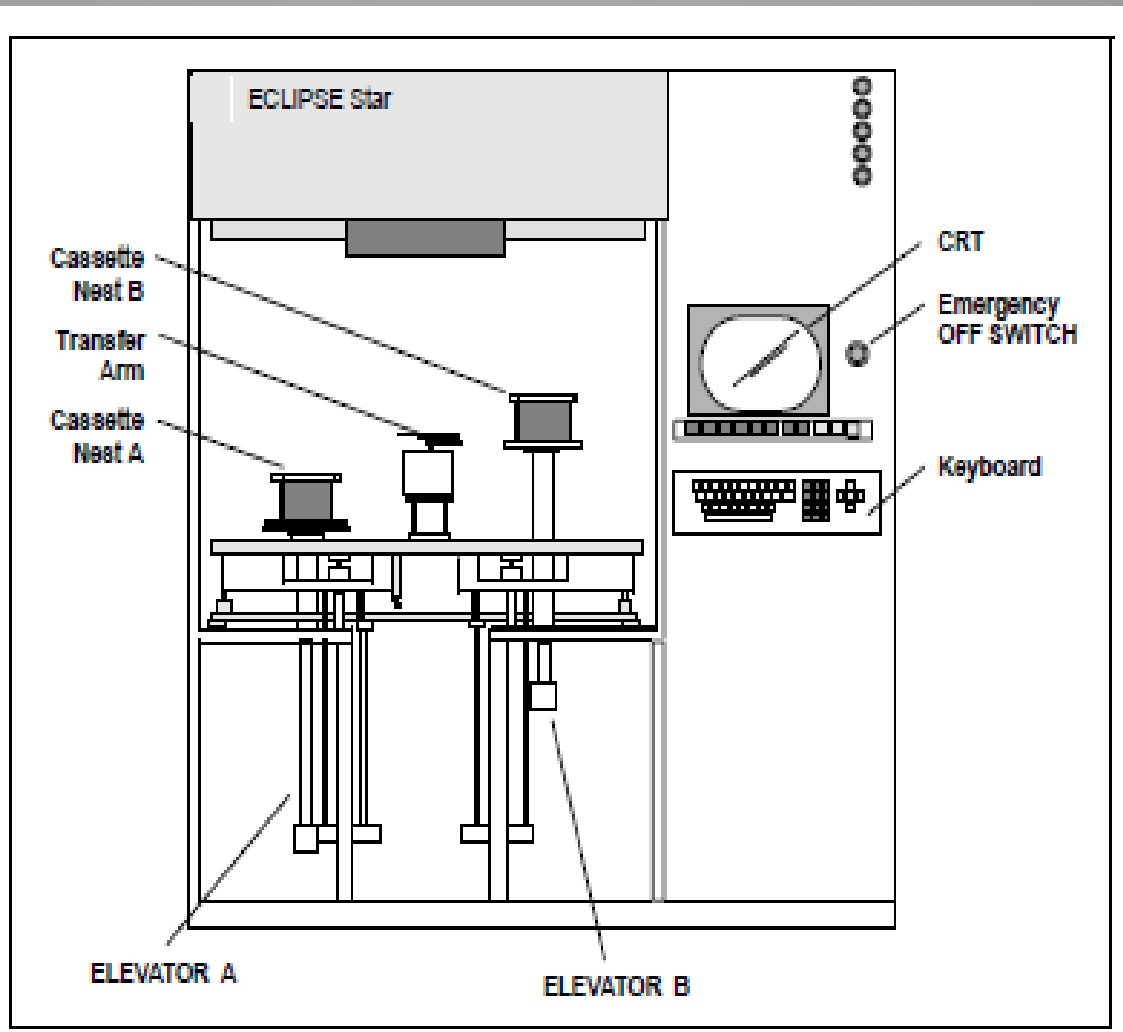
VARY	TO MAKE STRESS MORE COMPRESSIVE	TENSILE
Power/Rate	↑	↓
Argon Pressure	↓	↑
Substrate Temperature	↓	↑
Film Thickness	↑	↓
Bias	↑	↓

2.2 System Placement - Dimensional Footprints

The ECLIPSE Star system footprint is 61-1/2 inches wide by 105-5/8 inches deep by 88-11/16 inches high. (Also, 156 cm wide by 268 cm deep by 225 cm high.)



a. Components can be placed on an optional stand assembly to save floor space (see Figure 2-5 on page 2-8).
b. Required service area.


ECLIPSE Star
Cassette Neat B
Transfer Arm
Cassette Neat A
CRT
Emergency OFF SWITCH
Keyboard
ELEVATOR A
ELEVATOR B

Cathode	Hard Etch	Soft Etch
Etch Rate (Å/min)	100< x <250	100< x <600
Etch Unif, WiW, % 1 sigma	<5.0	<5.0
Etch Unif, WtW, % 1 sigma	<2.5	<5.0
Particle Contribution		<0.10 p/cm2 >0.3 um
Process Conditions	Remove 350Å thermal oxide from 10000Å oxide wafer, 1000 volt, 50 sccm Ar, 300°C, throttled to 5.0 mtorr	Remove 350Å thermal oxide from 10000Å oxide wafer, 125 volts, 1000 watts, 50 sccm Ar, 300°C, throttled to .8 mtorr
Document / Version #	215-11-005-001 / 9411	215-11-005-002 / 9411

Cathode	RMX-10 Ti	RMX-12 Ti	SPA-10 Al	SPA-12 Al
Deposition Rate (Å/sec)	>50	>50	>200	>200
Resistivity (uohm-cm)	<60	<60	3.1 ± 0.1 (Al1Si.5Cu)	3.1 ± 0.1 (Al1Si.5Cu)
Rs Uniformity, WiW, % 1 sigma	<2.5	<1.5	<2.5	<2.0
Rs Uniformity, WtW, % 1 sigma	<1.0	<1.0	<1.0	<1.0
Thickness Uniformity, WiW, % h-l	<5.0	<5.0	<5.0	<5.0
Thickness Uniformity, WtW, % h-l	<2.0	<2.0	<1.5	<1.5
Reflectivity at 436 nm, %, Si = 100%	>120	>120	>190	>190
Reflectivity Uniformity, WiW, % 1 sigma	n/a	n/a	<1.0	<1.0
Reflectivity Uniformity, WtW, % 1 sigma	n/a	n/a	<1.0	<1.0
Stress (dynes/cm2)	<5E9T	<5E9T	<5E9T	<5E9T
Particle Contribution	<0.10 p/cm2 >0.3 um	<0.10 p/cm2 >0.3 um	<0.10 p/cm2 >0.5 um	<0.10 p/cm2 >0.5 um
Process Conditions	2000 Å thick film, 6kw, 100 sccm Ar, 300°C, throttle open at 2.7 mtorr	2000 Å thick film, 8kw, 100 sccm Ar, 300°C, throttle open at 2.7 mtorr	10000 Å thick film, power adjusted to maintain ~222 Å/sec, 100 sccm Ar, 300°C, throttle open at 2.7 mtorr	10000 Å thick film, power adjusted to maintain ~222 Å/sec, 100 sccm Ar, 300°C, throttle open at 2.7 mtorr
Document / Version #	215-11-005-003 / 9411	215-11-005-005 / 9411	215-11-005-007 / 9411	215-11-005-008 / 9411

Barrier Processes

Cathode	RMX-10 TiW	RMX-10 TiN	RMX-12 TiN
Deposition Rate (Å/sec)	>50	>20	>20
Resistivity (uohm-cm)	<75	<130	<120
Rs Uniformity, WiW, % 1 sigma	<2.5	<4.0	<2.5
Rs Uniformity, WtW, % 1 sigma	<1.0	<2.0	<1.5
Thickness Uniformity, WiW, % h-l	<5.0	<10.0	<5.0
Thickness Uniformity, WtW, % h-l	<2.0	<5.0	<5.0
Reflectivity at 436 nm, %, Si = 100%	110 to 120	45 to 55	45 to 55
Reflectivity Uniformity, WiW, % 1 sigma	n/a	n/a	n/a
Reflectivity Uniformity, WtW, % 1 sigma	n/a	n/a	n/a
Stress (dynes/cm2)	<8E9C	<2E10C	<2E10C
Particle Contribution	<0.15 p/cm2 >0.7 um	<0.15 p/cm2 >0.3 um	<0.15 p/cm2 >0.3 um
Process Conditions	1000 Å thick film, 4.0kw, 100°C, 100 sccm Ar, throttled to 5.0 mtorr	1200 Å thick film, 6kw, 300°C, 20 sccm Ar, 70 sccm N2, throttle open at 2.5 mtorr	1200Å thick film, 8kw, 300°C, 20 sccm Ar, throttle open, Sput 1 N2 = 55 sccm, Sput 2/3 N2 = 60 sccm, 10 sec sput delay
Document / Version #	215-11-005-004 / 9411	215-11-005-009 / 9411	215-11-005-006 / 9411

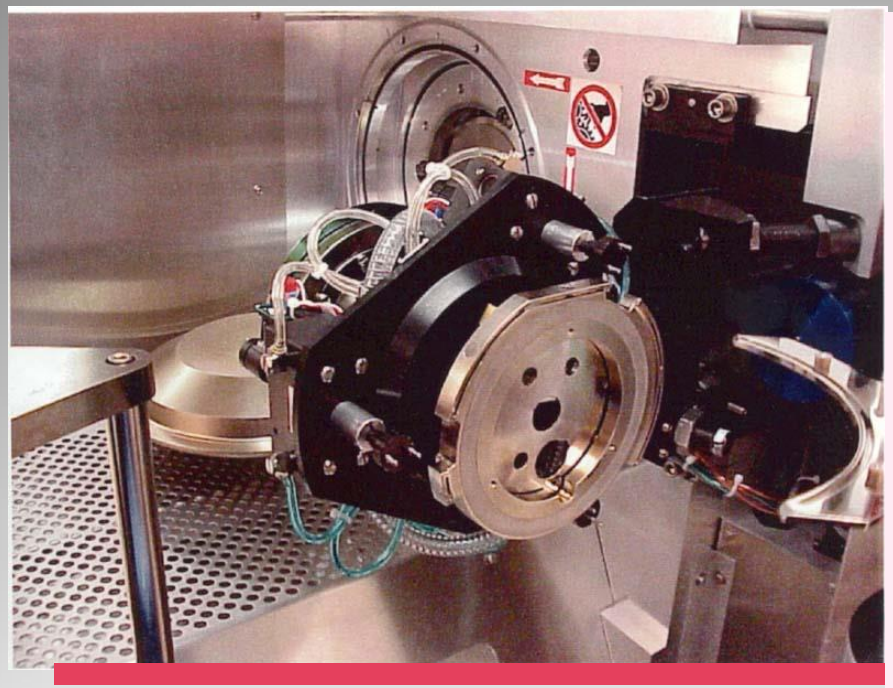
Anti Reflective Coating Process

Cathode	RMX-12 TiN
Rs Uniformity (%, 1 sigma, WiW)	<2.5
Rs Uniformity (%, 1 sigma, WtW)	<4.0
Reflectivity on Oxide (at 436nm, Si=100%)	60 to 100
Reflectivity Unif on oxide (%, 1 sigma, WiW)	<6.0
Reflectivity Unif on oxide (%, 1 sigma, WtW)	<6.0
Reflectivity on 1 um Al (at 436nm, Si=100%)	20 to 35
Reflectivity Uniformity on Al (%, 1 sigma, WiW)	<2.0
Reflectivity Uniformity on Al (%,1 sigma, WtW)	<2.0
Process Conditions	500Å thick film, 8kw, 300°C, 20 sccm Argon, throttle open, Sput 1 N2 = 55 sccm, Sput 2/3 N2 = 60 sccm, 10 sec sput delay
Document / Version #	215-11-005-006 / 9411

Eclipse for special application

Backside, Thin and Fragile Substrate Wafer Handling

Backside, Thin and Fragile Substrate Wafer Handling



- Wafer handling limited to outer 5mm of wafer device side
- Edge only contact optical pre-aligner
- System hardware optimized for maximum protection of device surface
- All metal processes supported, including high stress films
- Over 35 systems in backside/UBM, over 9 years manufacturing experience
- Front & backside deposition, standard thickness to 150µm thinned wafers

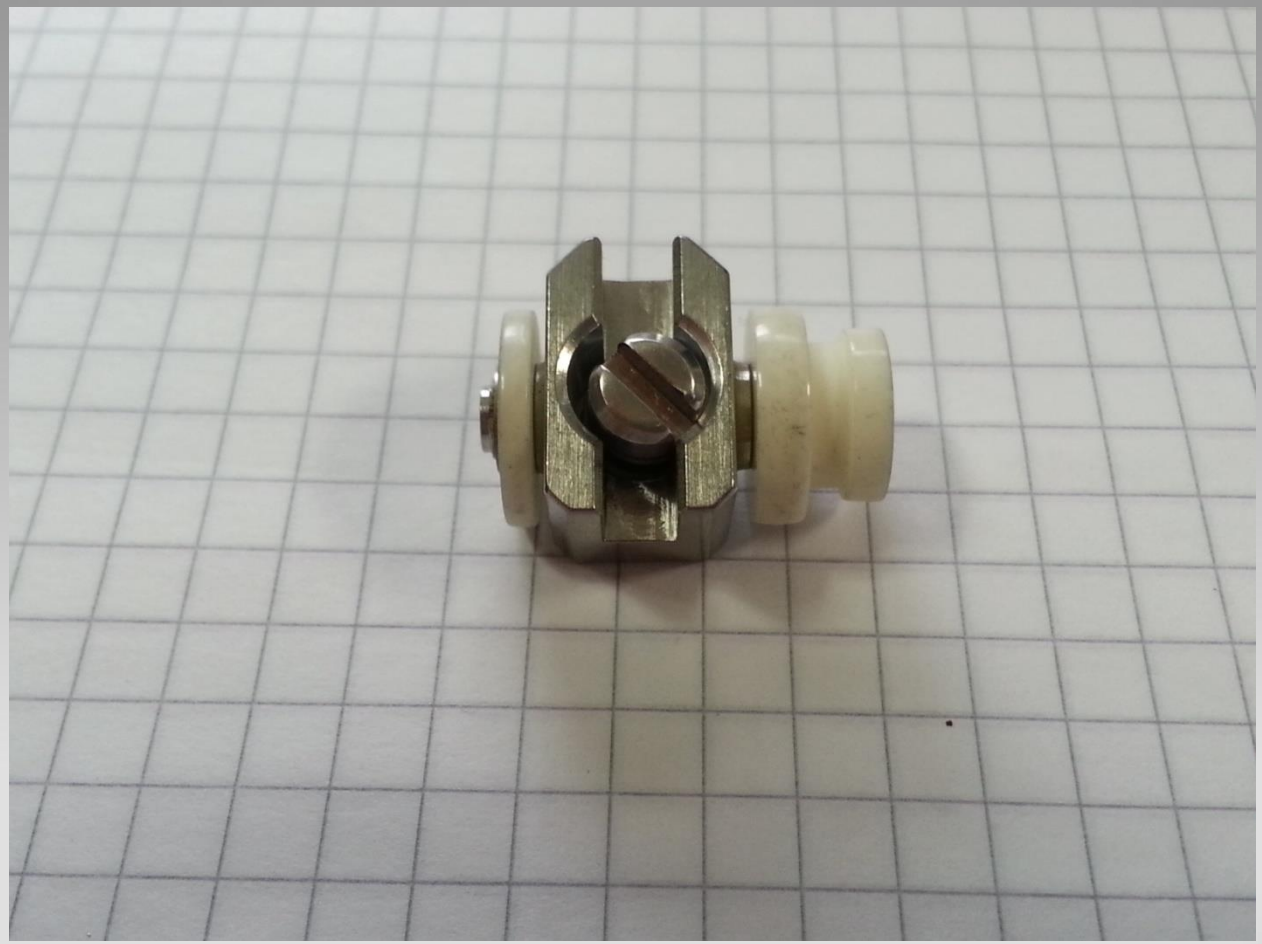
TFE suggested hardware for the Eclipse GaAs Two possibilities

Thin Film Equipment

Questions

- Notched or Flat wafers?
- Wafers thickness ?
- Heat during sputtering? What temperature?
- Etch before deposition? Soft or Hard Etch?
- What materials & thickness deposited?
- Where are the wafers broken ?
- How many wafers broken on 10000?
- Eclipse model & Front end type?

Stainless steel Latch with ceramic roller



Performance features/benefit

Performance Features/Benefits

- Excellent thermal stability
- Excellent chemical resistance
- Excellent compression set resistance
- Good response to temperature cycling effects

Typical O-ring Compression Set Performance* (70 hr data)

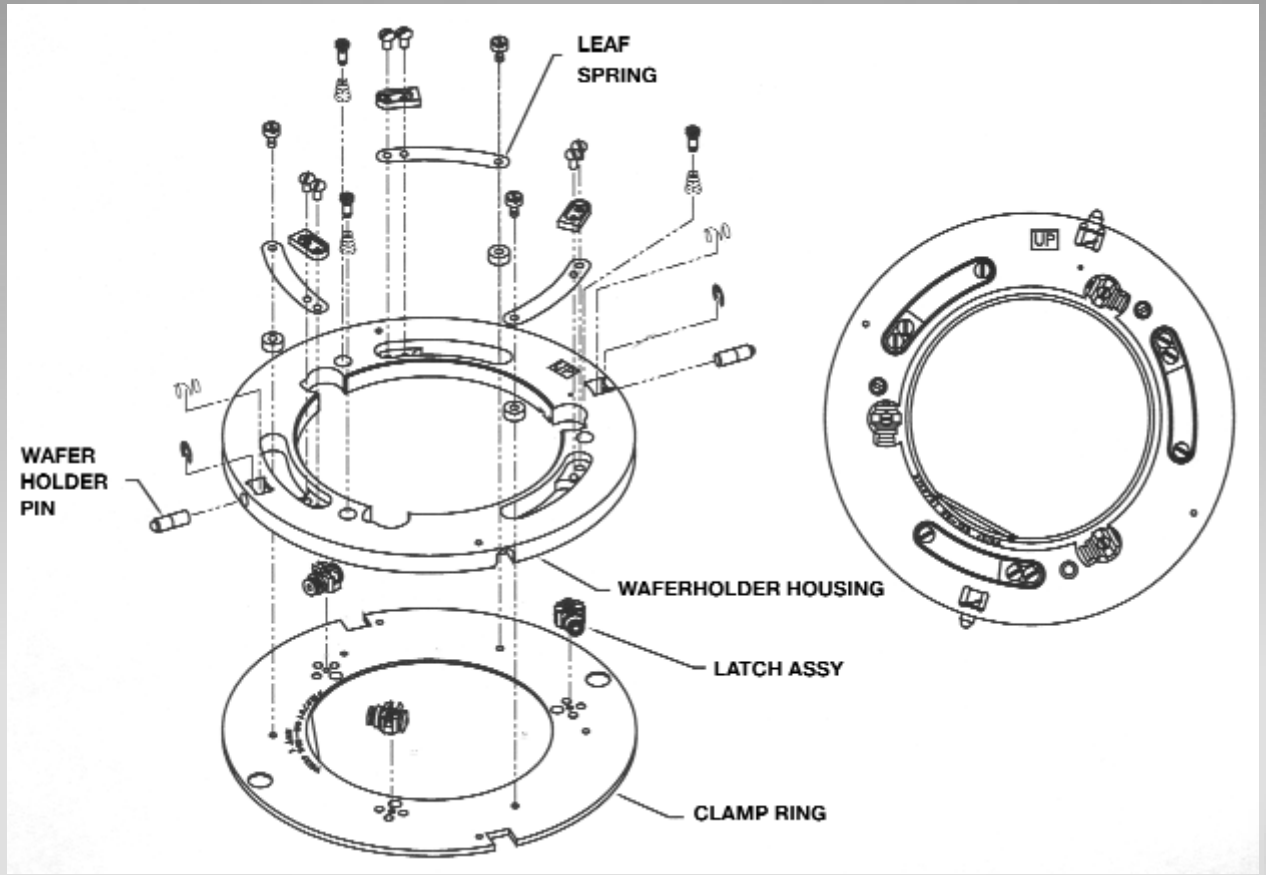
Material Tested, % C/S at	204°C	250°C	300°C
Kalrez® 4079	37	41	45
Competitive FFKM A2	43	100	Sample Failed

* ASTM D 395B and D 1414 (AS568 K214 O-ring test specimens)

Typical Physical Properties[1]	
Hardness Shore A, (pellet)[2]	75
Hardness Shore M, (O-ring)[3]	83
100% Modulus[4], MPa	7.23
Tensile Strength at Break[4], MPa	16.88
Elongation at Break[4], %	150
Compression Set[5], % 70 hr at 204°C, %	25
Max Continuous Service Temperature[6], °C	316

[1] Not to be used for specification purposes
[2] ASTM D 2240 (pellet test specimens)
[3] ASTM D 2240 and ASTM D1414 (AS568 K214 O-ring test specimens)
[4] ASTM D 412 (dumbbell test specimens)
[5] ASTM D 395B (pellet test specimens)
[6] DuPont Performance Elastomers proprietary te

Current Wafer Holder/Clamp Ring Design



Hard Etch

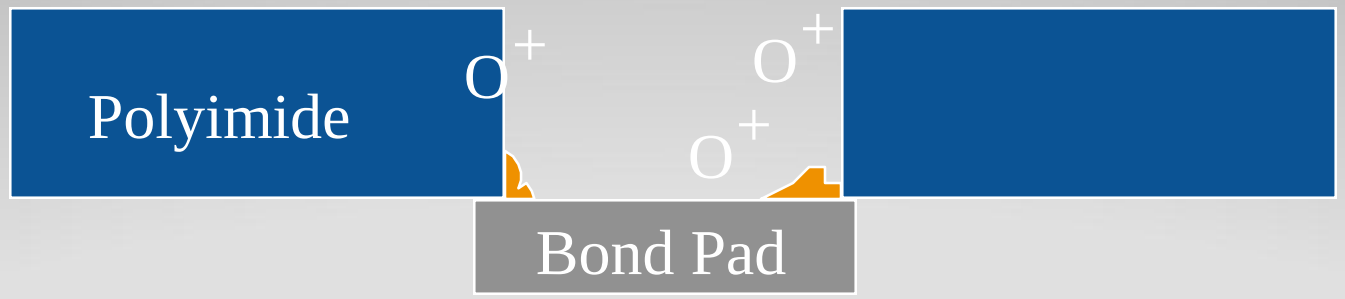
- Moderate etch rate
- High RF bias voltage
- Low particulate process chamber
- RF diode etch
- Ideally suited for applications where large areas of exposed metal and/or silicon are present

ICP Preclean
Turbo Pump Option

- CTI Turbo Plus Package
- Enables the use of reactive gases
- Chamber/Bell Jar Cleaning
  - Using an ICP only plasma with Ar/O_2.
  - Removes residual polyimide from the bell jar and shielding.
  - Re-oxidizes the bell jar; Self conditioning.
  - Used with Al shielding; Self conditioning.
  - Extends bell jar lifetime

Residual Photo Resist or Polymer Removal

- Use an Ar/O_2 ICP plasma along with RF etch.
- Will aid in passivating polyimide surface.
- Process is “Self-Cleaning.”



Contamination Removal

- Residues from final via etch (Fluorides)
- Identify chemistries that produce pump friendly reaction products.
- Design reaction mechanisms to create products with low sticking coefficients.
- Promote fluorinated molecule formation:
  - Use Inductively Coupled Plasma Only
  - Reactive Process Gas Types: Ar/H_2, NH_3, NO_2

Suggested Process Sequence

- Step 1: Use an Ar/H_2 ICP plasma to remove fluorine contamination.
- Step 2: Use Ar/O_2 Soft Etch process (ICP+RF) to clean residual photoresist.
- Step 3: Purge O_2 , using Ar only.
- Step 4: ICP Soft Etch process; Clean the oxidized bond pad.

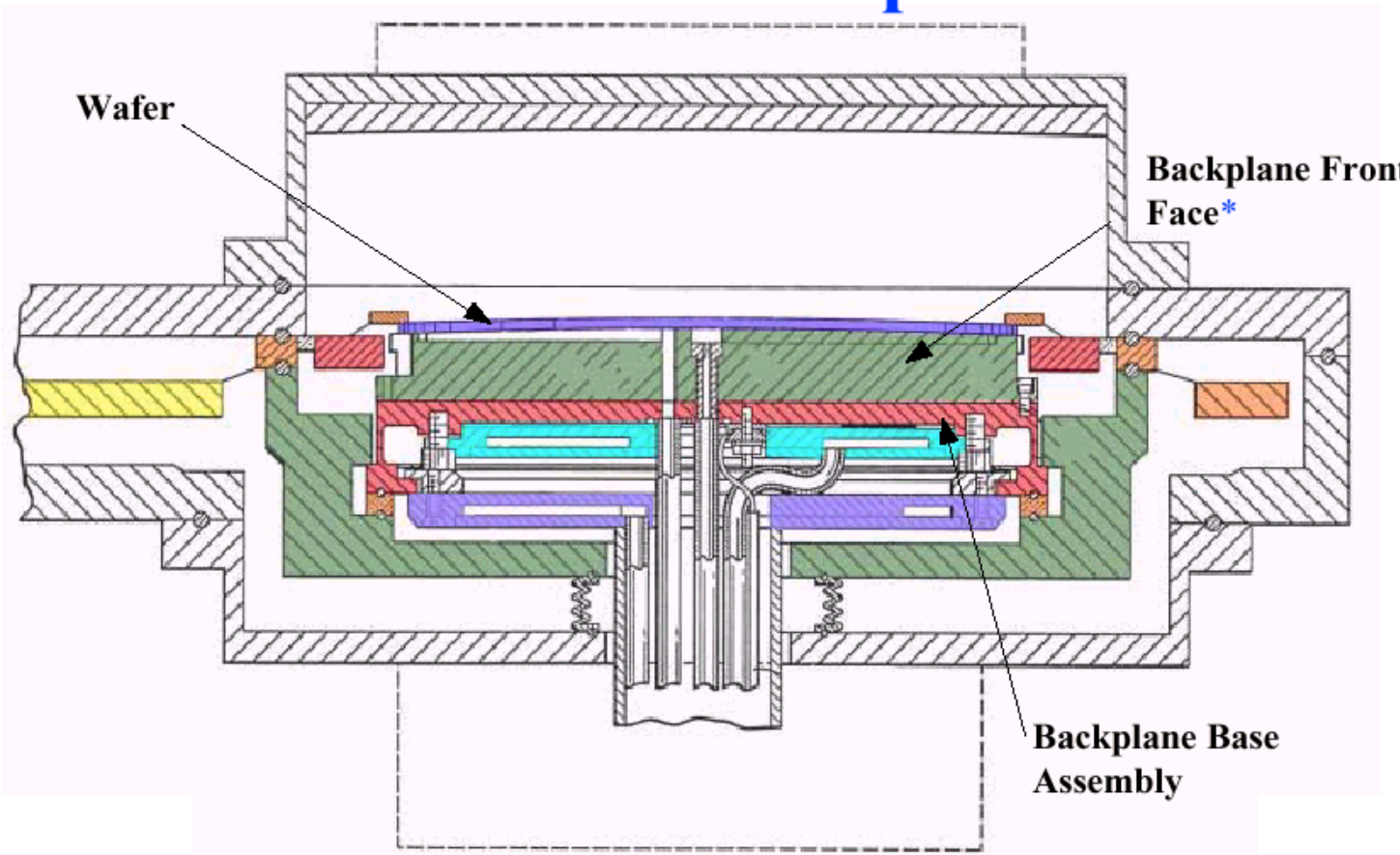
Turbo Pump Upgrade Summary

- Allows alternate plasma chemistries to decontaminate inbound wafers and chamber.
- Dramatically increases throughput
  - Typical contamination reduction by pumpout only: 5 min
  - With reactive preclean: < 2.5 min
- Theoretical bell jar lifetime is months, not days (as long as deposition is oxide or carbon based).
- Allows chamber to be conditioned without using multiple oxide wafers.

Universal Backplane

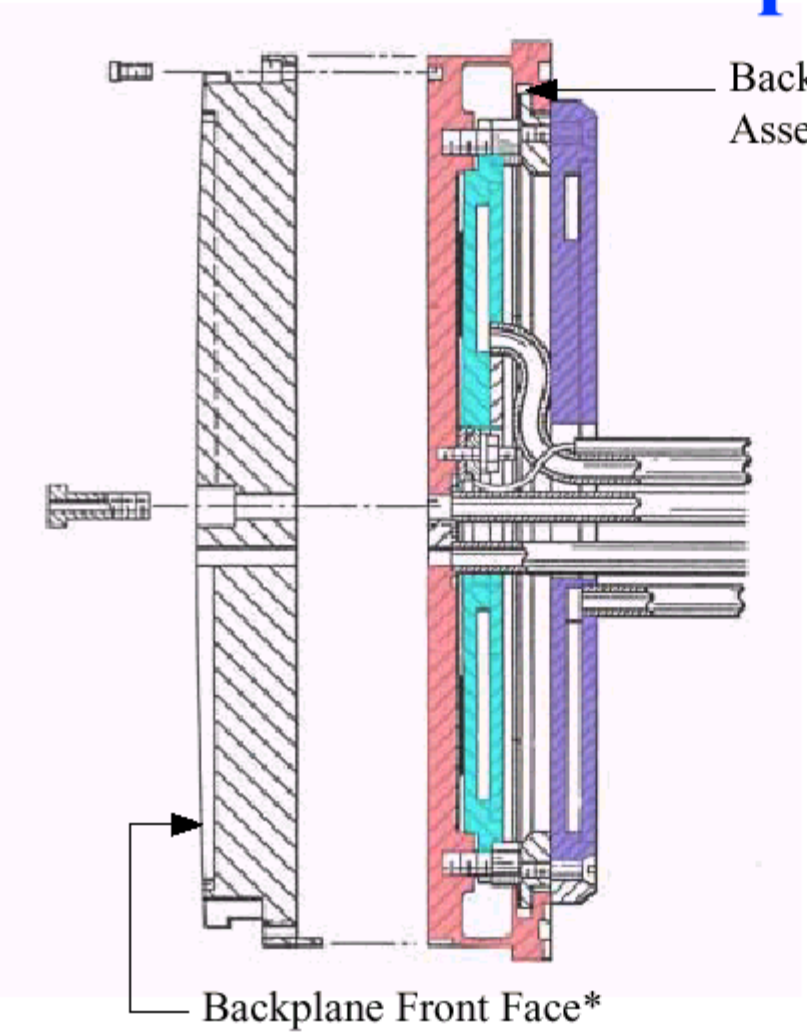
- Provides capability for reduced time in converting tools from one wafer size to another.
  - Time reduced significantly.
    - Dependent on system configuration, process operating conditions, reclamation procedures & customer specific operating procedures.
  - Available in 4”, 5”, 6” and 8” sizes.
    - Both contact and non-contact applications.

Universal Backplane



* Wafer Size Dependent

Universal Backplane



* Wafer Size Dependent

Collimated Liner Processes

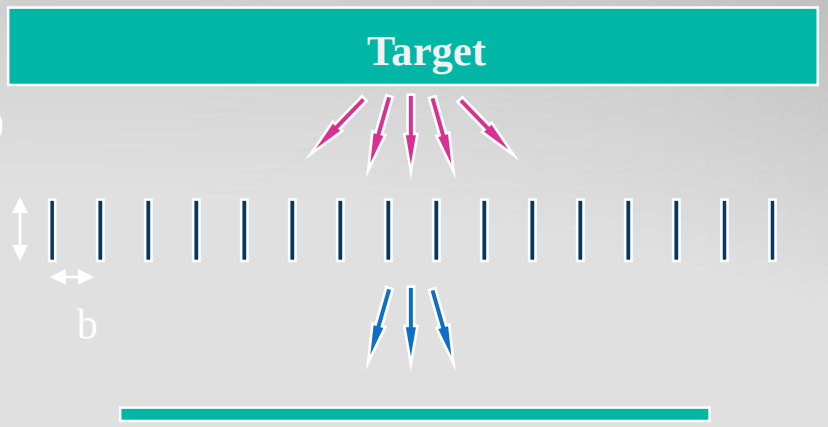
Collimation improves fill by removing sputtered flux with large incident angles

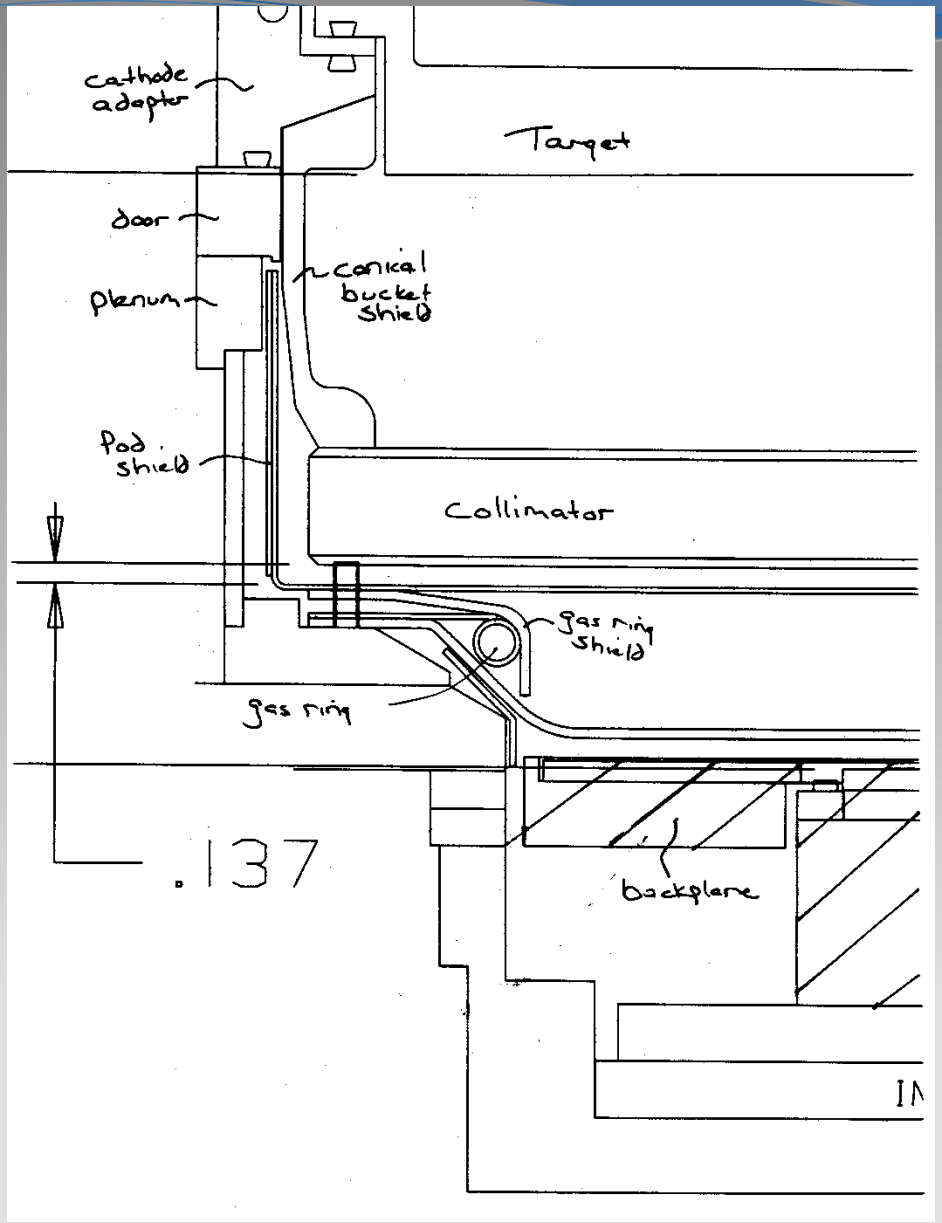
ICC-12 Cathode designed for optimum film uniformity and long kit life

30 kW max. Ti process with ARO to maintain constant high throughput

Collimator Aspect Ratio

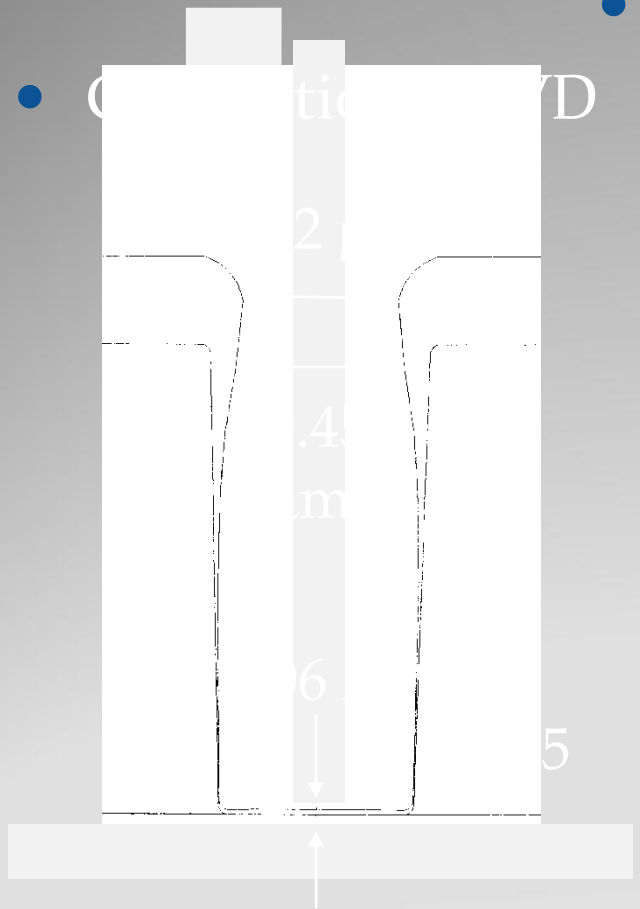
AR= a / b

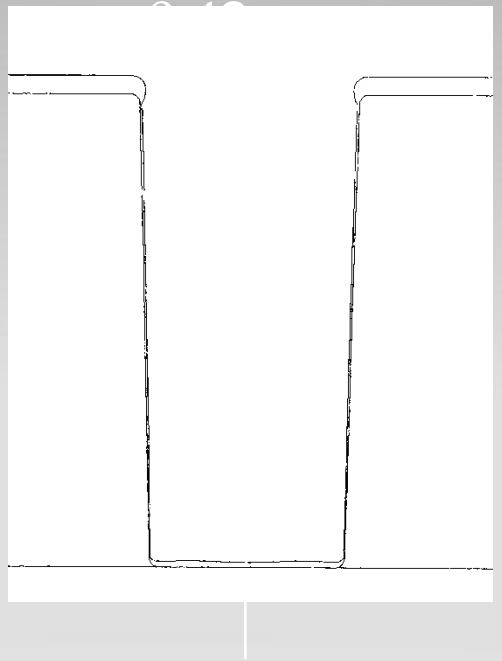


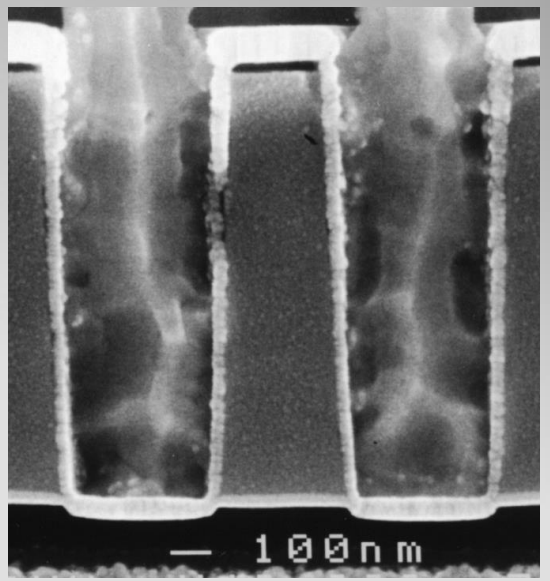

cathode adapter
Target
door
plenum
conical bucket shield
Pod shield
Collimator
gas ring shield
gas ring
.137
backplane

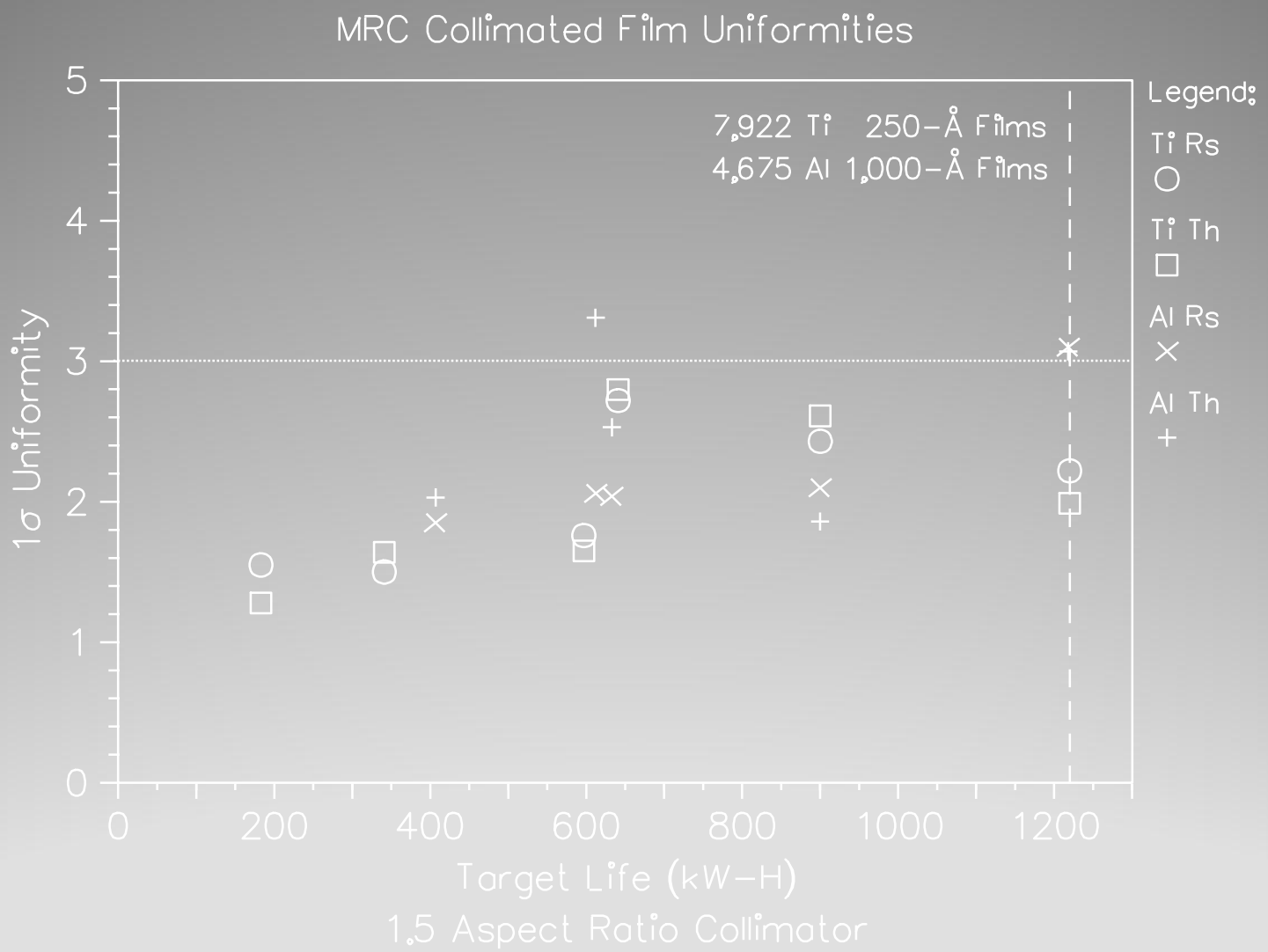
Directional Deposition Solves Feature Close Off Problem

- Feature: 0.4 μm, 2.4 AR, 88.5° walls
- Deposition Method
  - C[illegible]ti[illegible]VD
  - Collimated PVD
  - coll. Ti/TiN/Ti








MRC Collimated Film Uniformities
7,922 Ti 250-Å Films
4,675 Al 1,000-Å Films
Legend:
Ti Rs
Ti Th
Al Rs
Al Th
1σ Uniformity
0
1
2
3
4
5
0
200
400
600
800
1000
1200
Target Life (kW-H)
1.5 Aspect Ratio Collimator

Eclipse Wafer Temperature

Eclipse Wafer Temperature

- Control is achieved by using backside gas
  - Heat source (bring wafer temp. up/down)
  - Heat sink (hold wafer temp. during dep.)
- Without control, deposition of 1 µm of Al
  - raises wafer temperature by 250 - 550 C
  - wafer is only inefficiently cooled by radiation
- Understanding of the mechanism is key for
  - successful process design on the Eclipse
  - successful process move from/to „other“ equipment

Eclipse® Mark™ IV

Clamp Ring Options

Given to AMD Dresden in 2000

And MOS3 Nijmegen 08/2001

TEL Mark IV Clamp Ring Discussions

- Clamp Ring Requirements
- Current Clamp Ring Design
- Alternate Clamp Ring Options
- Discussions/Conclusions

Eclipse® Mark™ IV

GaAs Applications

General GaAs Metallization Processes

- Ohmic Metals
  - Ni, W, Ge, AuGe, AuGeNi, AuZn
- Schottky Barriers
  - Ti, TiW, TiWN, Ta, TaN
- Resistor Films
  - TaN, NiCr, SiCr
- Interconnects
  - Au, Al

Currently no process experience with Ge and Ge alloys in Eclipse Systems

Eclipse® Mark™ IV

GaAs Key Advantages

Eclipse Unique Features

- Identified for the Osram OS new fab project in Burgweinting
  - General
  - Technology
  - Cost and Operation

Eclipse Unique Features - General

- TEL is a world class semiconductor equipment supplier
  - Solid local service, parts and process support
- Eclipse is a mature equipment family with a large installed base (> 350 systems)
  - solid installed base in GaAs and other fragile substrate technologies
  - long process experience with a wide range of materials
  - Mark IV is fully up-to-date in hardware, automation and process technology
  - TEL committment to further development of the Eclipse family

Eclipse Unique Features - Process

- Tight wafer temperature control with contact backplanes
  - still some temperature control with non-contact backplane
- Vacuum isolated UHV chambers for reactive processing
  - high gas conductance chambers for fast pumpout
- Choice of two preclean technologies (Hard Etch + ICP PC)
- Wide material flexibility with only two cathode types
  - material change requires only target and shield change
  - multipass option for material sequence flexibility
- Unique, production-proven fragile substrate handling kit
  - wafer breakage specification = 1 / 3000

Eclipse Unique Features - COO Op.

- Almost full Gold reclaiming from optimized shields
  - Gold consumption for one target life (1600 µm dep.): 861 g on produ wafers (150mm), 162 g lost, everything else reclaimed
- Equipment designed for lowest COO
  - small footprint, compact design
  - high throughput (up to 50 waf/h) serial wafer index
  - two-piece shields and quick target change kits
  - universal hardware for quick wafer size conversion (4 h)
- SECS-GEM automation and full grahical user interface
- Dedicated pre-process cassette and ARO features
  - automatic conditioning and power/time correction

Eclipse® Mark™ IV

for MOEMS

Metalization Process Sources

MEMS and MOEMS (Optoelectronics) use production-proven process modules where possible

In-device interconnects

- mainstream DRAM and µProc processes

Bonding/Packaging interconnects

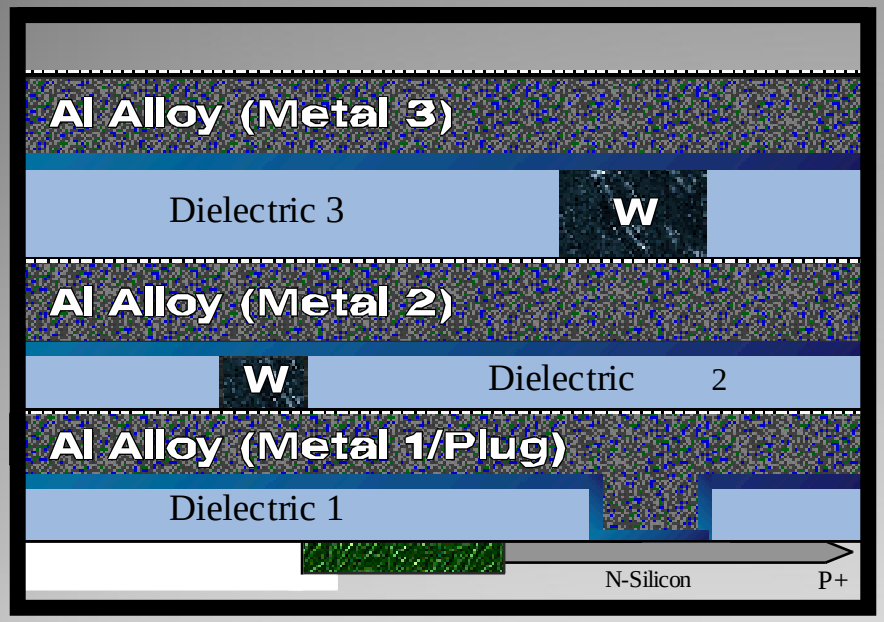
- mainstream Packaging and UBM stacks
- often used also in-device for process simplicity

Resistors (Resistive Heaters)

- MEMS
- Inkjet Print Head materials

Eclipse® Mark™ IV

Al Interconnects - Slab for 150/200mm wafers

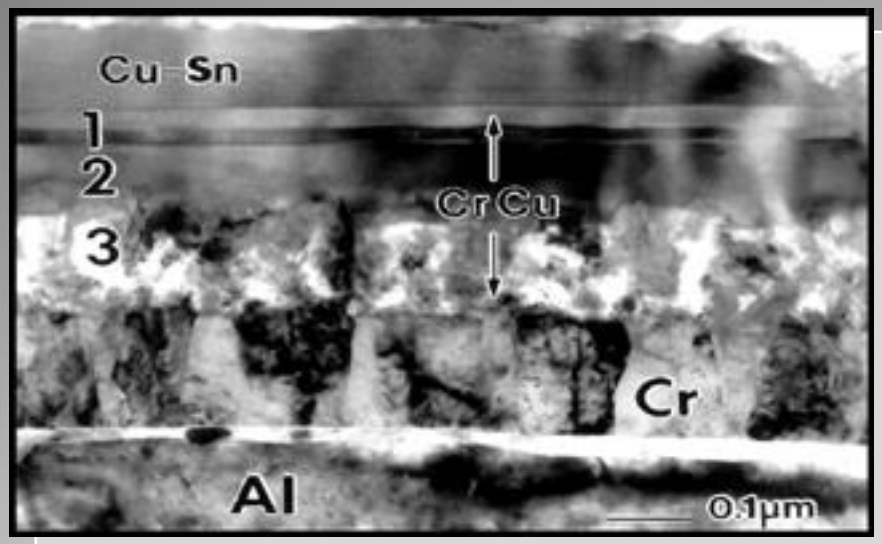


Schematic of 3 metal levels using Al Plug, W Plug and Slab Al

- Example:
- 200mm global wiring for 0.5 µm node

Process	Thickness	Rate	Unif. 1σ
SE	(200)Å	>7Å /sec	<8.0%
Ti	300Å	>50Å/sec	<2.1%
Al	1 µm	>190Å/sec	<2.0%
TiN	400Å	>20Å/sec	<3.5%

C-4 Packaging Application

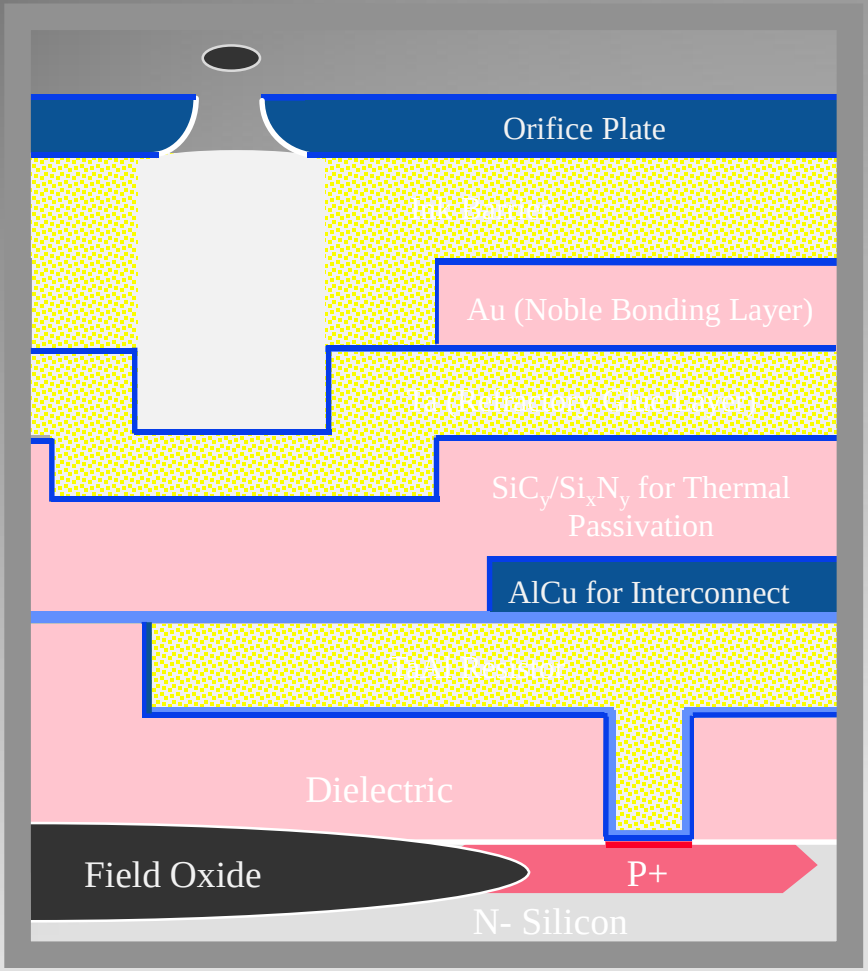


Cross-sectional SEM of typical C-4 liner stack

- Example:
- Typical 200mm Production Process

Process	Thickness	Rate	Unif. 1σ
SE	(200)Å	>7Å/sec	<8.0%
Cr	2000Å	>25Å/sec	<3.0%
CrCu	2000Å	>30Å/sec	<3.0%
Cu	5000Å	>120Å/sec	<2.5%

Inkjet Metallization - Slab Wiring for Printer Heads

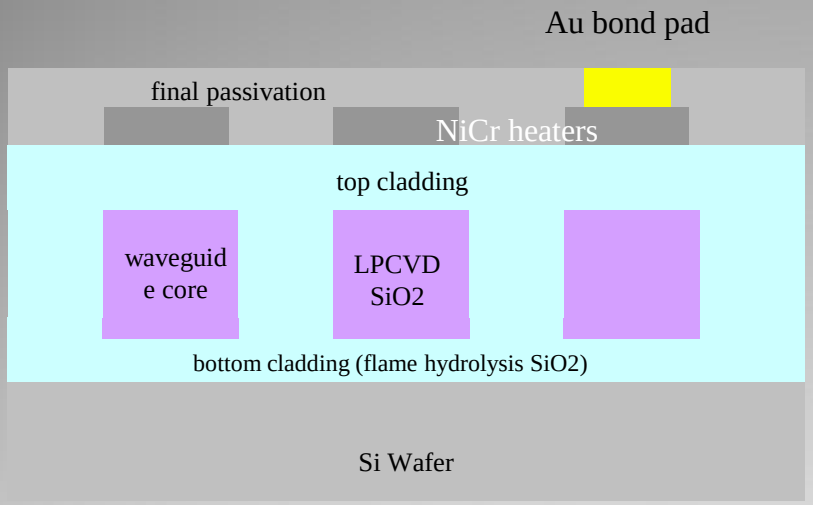


- Example:
- 150mm Production Process

Process	Thickness	Rate	Unif. 1σ
ICP SE	(200)Å	>7Å/sec	<8.0%
Ta	3500Å	>80Å/sec	<1.5%
TaAl	800Å	>60Å/sec	<2.0%
Au	5000Å	>150Å/sec	<3.0%

Schematic of Inkjet interconnect structure

Optoelectronic resistive heater and bond pad



- Example:
- 200mm Production Process

Process	Thickness	Rate	Unif. 1σ
NiCr	2.4μm	>90Å/sec	<2.5%
Au	5000Å	>150Å/sec	<3.0%

Other Advantages:

NiCr process optimized for low stress layer (RF bias + ...)

Specific Requirements for MOEMS and Optoelectronics

- Interconnects on-chip and for packaging
  - large structures often require high currents
  - thicker films,
  - adhesion (stress) more critical
- Resistor films
  - large devices make within wafer uniformity more critical
- Your Requirements ?

Comparison of Metallization Processing Techniques

- Evaporation
- Batch Sputtering
- Single Wafer Deposition

Evaporation

- Multiple processing steps
- Low throughput which decreases with increasing wafer size
- High evaporation non-uniformity due to angular source flux (diffused emission)
- No substrate temperature control
- Difficult to reclaim precious metals, i.e. Au
- Manual wafer handling

Batch Sputter Systems

Low throughput which decreases with increasing wafer size

High non-uniformity

Low vacuum results in poor film quality

- Large percentage of film oxidized which can increase device current and decrease reliability

No substrate temperature control

Potential target cross-contamination for reactive processing

Manual wafer handling

Modern Single Wafer PVD Systems

Cassette-to-cassette automated wafer handling

Throughput is not dependent on wafer size

Substrate temperature control (not all!)

Ultra high vacuum (UHV) system

- Better device reliability, repeatability of films

Non-uniformity is lower than evaporator and batch systems

- WiW: < 3% 1σ; WtW: <1.5% 1σ

Vacuum Isolated Process Chambers (not all!)

- allow reactive sputtering

Advantages of Eclipse® Sputter System

Excellent Film Stress Control

- tight wafer temperature control
- RF/DC bias capability
- wide pressure operating range

Full set of mass-production features

- operation, automation, maintenance
- High throughput: up to 50 wafers/hour
- Special Handling Features for Fragile Substrates
- 1:1 transfer of developed process into production

Vertical Sputtering reduces >5µm particles

TEL Experience in PVD Films

Over 40 years of accumulated experience in materials and film deposition

- process transfer from batch/research systems

Very Experienced Field Process Support

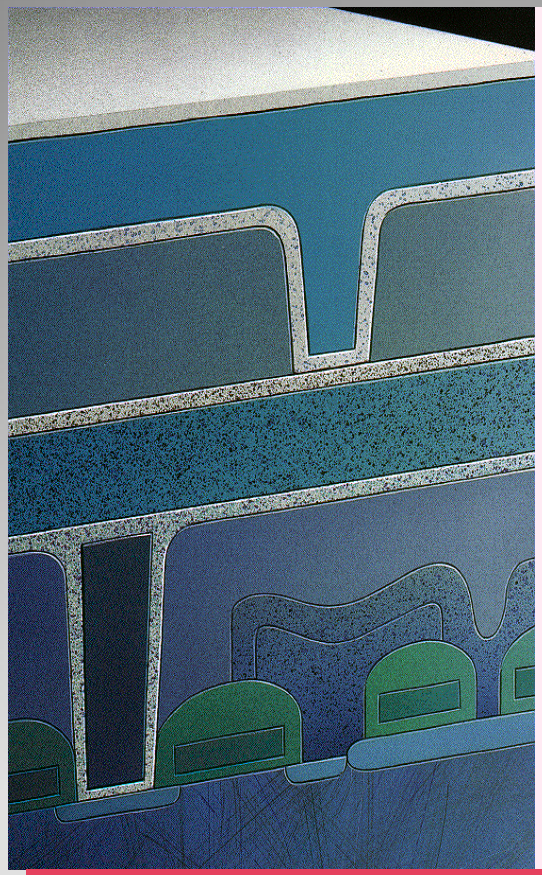
- average of 12 years in microelectronics

Unique Range of field-proven Applications

Applications Laboratory in Phoenix, AZ

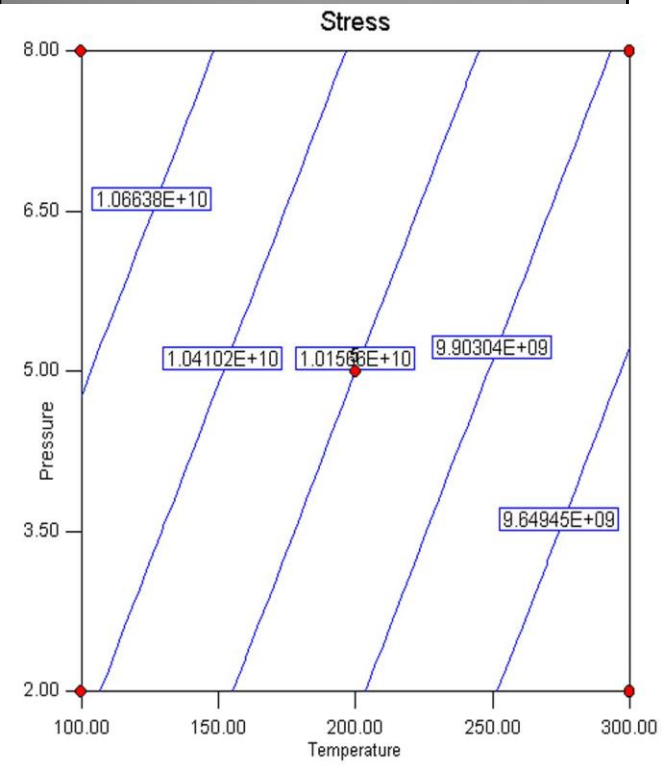
- process development
- feasibility studies
- demo capability

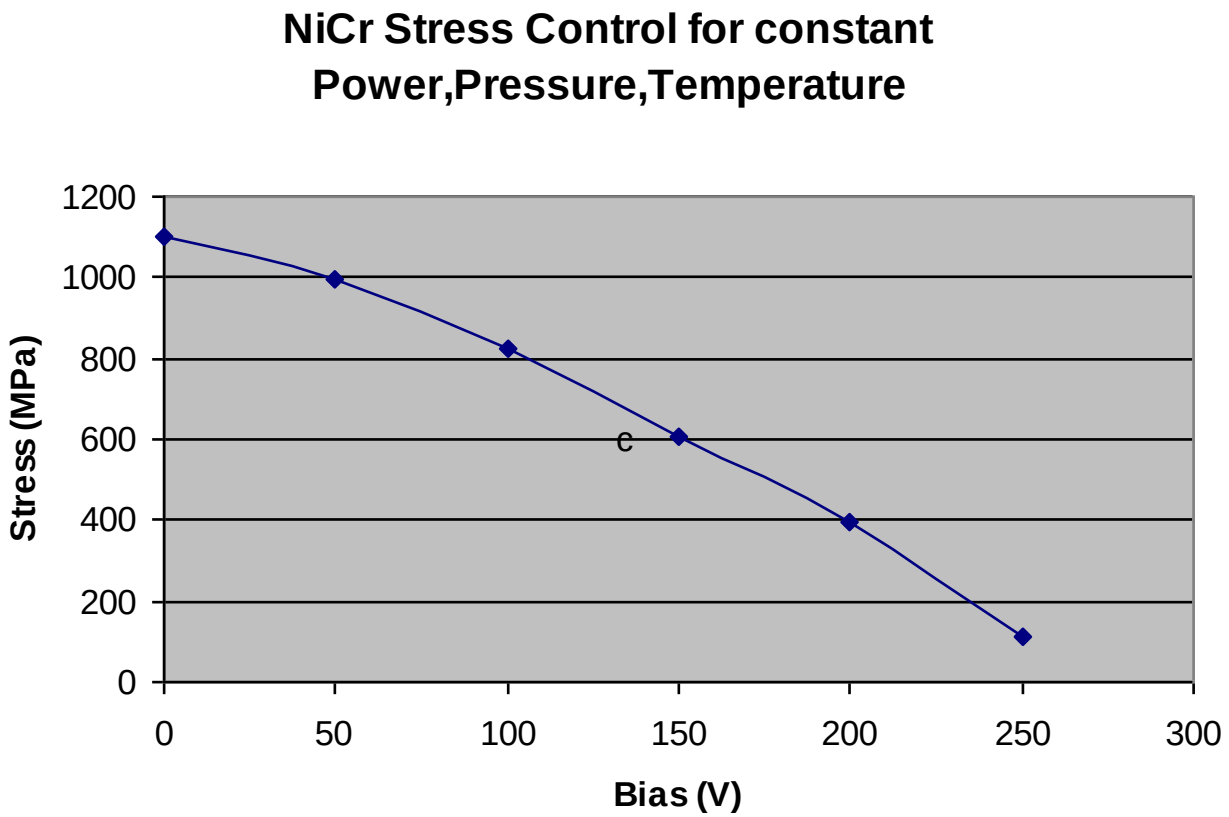
Eclipse® Mark™ IV Integrated Applications



- Interconnects
  - Ti, TiN, Al, TiN and Hot Al for via fill
- Barriers
  - TiN, TiON, TiW, TiWN, Co-TiN, Co-Ta, Ta, TaN and CoTaN
- Silicides
  - Ti, Co, Pt, WSi and Co-Ti
- Packaging (C-4 & Backside)
  - Ti, Cr, Ni, TiW, NiV, NiVN, CrCu, Cu, Au
- GaAs and Discretes
  - Cr, Ti, TiW, TiWN, Al, Pt, Au, Ag, Ta, Ni
- Resistors (Inkjet and Optoelectronics)
  - SiCr, NiCr, Ta, TaN, TaAl
- Conductors (Inkjet and Optoelectronics)
  - TaAl, Ta, Al, Au, Cu

Example: Resistor Stress Control





ICP Preclean

Specifications

	150mm	200mm
Bell Jar Material	Quartz	Quartz
Etch Rate (Å/min)	>100, <600	>100, <600
Etch Uniformity, WiW, % 1σ	<10.0%	<10.0%
Rs Uniformity, WtW, % 1σ	<2.5	<2.5
Argon (sccm)	25	25
Temperature (°C)	300	300
ICP Power/Bias	1000W / 100V	1000W / 100V
Chamber Pressure (mTorr)	0.8	0.8
Plasma Power Source	ICP	ICP

Preclean Process Issues

- optimize etch removal for optimal throughput and bell jar life
- SiC etching compromises process performance and process kit life
- efficient bell jar conditioning recipes extend kit life and avoid RF errors
- new particle spec for SiC etching in development
- setup-specific BKMs (Best Known Methods) available

Ion Bombardment

- Intense ion bombardment can reverse the effect of high gas pressure, i.e., zone 1 becomes zone T, i.e., more dense.
  - Eroding surface roughness i.e., reducing shadowing effects.
  - Creating new nucleation sites for arriving atoms.
  - The ion bombardment for aforementioned effect is very large ~30-36% eliminates shadowing.
  - Differential bombardment due to topography shadowing
  - At low deposition temperatures high energy ions tend to become trapped in the growing film.
  - Low energy ion are effective in removing impurities adsorbed on the surface and the growing film is cleaner.

Comparison of PVD Technologies

Comparison of Metallization Processing Techniques

- Evaporation
- Batch Sputtering
- Single Wafer Sputter Deposition

Evaporation

- still widely used
- Multiple processing steps
- Low throughput which decreases with increasing wafer size
- High evaporation non-uniformity due to angular source flux (diffused emission)
- No substrate temperature control
- Difficult to fully reclaim precious metals
- Manual wafer handling

Batch Sputter Systems

Low throughput which decreases with increasing wafer size

High non-uniformity

Low vacuum results in poor film quality

- Large percentage of film oxidized which can increase device current and decrease reliability

No substrate temperature control

Potential target cross-contamination

Manual wafer handling

Difficult to fully reclaim precious metals

Advantages of Eclipse® Sputter System

Cassette-to-cassette automated wafer handling

Throughput up to 50 waf/h, independent of wafer size

Substrate temperature control

Ultra high vacuum (UHV) system

- Better device reliability

Non-uniformity is lower than evaporator and batch systems

- WiW: < 3% 1σ; WtW: <1.5% 1σ

Less than 2% loss of precious metals

Precious Metal Economy

Gold Reclaim Data (real life) from Customer X						
Configuration: Mark II , 2.5mm EE clamp ring, funnel (reclaim) shield						
150mm wafers, 0.6µm Au/wafer, full thickness target (=2667 wafers/target)						
Au on new target (RMX-10)		8800	g	100%		
Au remaining on spent target		4889	g	55.60%		
= Au sputtered		3911	g	44.40%		
Au reclaimed from shields		2888	g	32.80%		
= Gold consumed		1023	g	11.60%		
Gold on product wafers		861	g	9.80%		
= Gold lost		162	g	1.80%		

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